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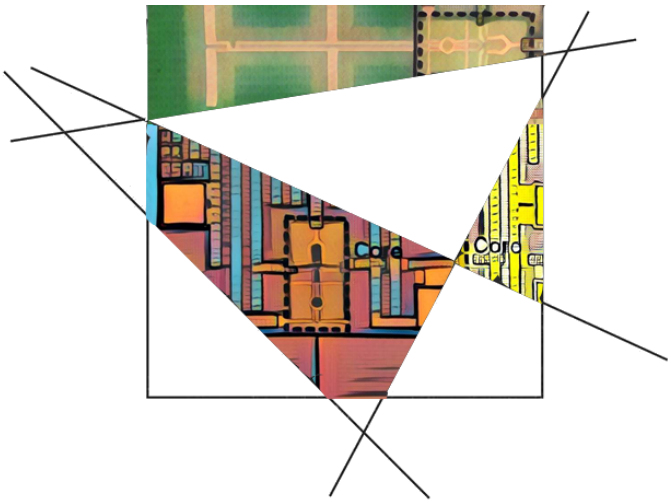
Faculty of Engineering Science
Department of Electrical Engineering

THz electronics design in nanometer CMOS



Wouter STEYAERT

Promoter:
Prof. dr. ir. ing. P. Reynaert

Dissertation presented in partial fulfillment of the requirements for the degree of Doctor of Engineering Science (PhD): Electrical Engineering

August 2017

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Voorwoord

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Wouter
B02.24, Heverlee, Somewhere in 2017

Abstract

Over the past 150 years, mankind has been able to cover large portions of the electromagnetic spectrum, ranging from the kilohertz radio waves up to exahertz gamma rays. One part of the spectrum, however, has remained elusive: the frequency range from 300GHz to 3THz, also referred to as the sub-mm wave or terahertz (THz) spectrum. Located on the intersection between microwaves (electronics) and IR/light (optics), the THz waves exhibit many unique and useful properties that can result in a wide variety of applications: Tbps communication links due to the large available bandwidth, non-destructive testing thanks to the transparancy of dielectrics at THz frequency, humidity sensors and spectroscopy because of molecular absorption and interaction, safe bio-medical imagers due to the non-ionizing THz radiation, ...

While the advantages and potential applications are clear, commercialization and usage of THz remains virtually absent. The THz spectrum proved to be too high frequency for all but the most advanced and expensive III-V technologies, while having a large wavelength only reachable by cryogenically cooled quantum-cascade lasers, resulting in the infamous 'THz gap' due to the lack of signal generator and receiver devices.

Over the past decade, the advancements of the CMOS process has yielded transistors able to operate at mm-wave frequencies. Although CMOS transistors do not support fundamental oscillation and amplification at THz frequency due to the limitations of f_{max}, the use of harmonics would allow to bypass this seemingly fundamental obstacle.

In this work, we present our research results towards the design and fabrication of fully integrated THz CMOS electronics with on-chip antennas. By utilizing below-f_{max} signals to generate above-f_{max} harmonics, signal generators from 0.54THz till 0.61THz have been implemented in deep-scale nanometer CMOS technology and measured. Fundamental oscillators are used to drive a non-linear, third harmonic-generating amplifier connected to probe pads and on-chip antennas. Using parasitic-aware design and extensive EM and transistor modeling and simulation, state-of-the-art operating frequency, bandwidth and chip area have been realized while maintaining a lensless, low-cost package. The integration of various on-chip antennas (dipole, folded dipole, collinear broadside dipole array) together with the signal sources results in THz radiators suitable for high-density sensor arrays. Various imaging measurements are presented utilizing the fabricated THz signal generators, illustrating the feasibility of THz CMOS for dielectric contrast imaging. Of these imaging experiments, a

non-destructive, contactless water content detector as well as the sub-mm spatial resolution verification of packaged surgical needles are noteworthy applications with real industrial potential.

In-depth analysis of the high-frequency performance of both transistors and passives in CMOS have been conducted and reported. A preliminary study on the compatibility and impact of several antenna types and packaging methods for THz electronics is given, in addition to an overview of current state-of-the-art circuits and applications that could benefit from a low-cost, mass producible implementation in CMOS.

Injection-locked dividers, super-regenerative receivers (SRR) and Schottky barrier diode (SBD) detectors have been investigated as potential THz receiver circuits. A 0.58THz SRR with flipchip dipole antenna in 28nm CMOS is implemented, as well as SBDs with on-chip bowtie antennas for broadband 0.5THz-1THz detection. A 30THz on-chip bowtie antenna is designed, targeting the long-infrared spectrum for thermal imaging applications.

Samenvatting

De afgelopen 150 jaar heeft de mensheid grote delen van het elektromagnetische spectrum kunnen ontdekken, gaande van kilohertz radiogolven tot exahertz gammastraling. Een deel van het spectrum blijft echter buiten bereik: de frequentieband van 300GHz tot 3THz, ook wel het sub-mm golf of terahertz (THz) spectrum genoemd. Deze THz-golven bevinden zich op het snijpunt van microgolven (elektronica) en IR/licht (optica), en hebben veel unieke en nuttige eigenschappen die kunnen leiden tot een breed scala aan toepassingen: Tbps-communicatieverbindingen door de grote beschikbare bandbreedte, niet-destructieve testen dankzij de transparantie van dielectrica op THz frequentie, vochtigheidssensoren en spectroscopie door de moleculaire absorptie en interactie met THz-golven, veilige biomedische beeldvormers door de niet-ioniserende THz-straling,...

Terwijl de voordelen en potentiële toepassingen duidelijk zijn, blijft commercialisering en gebruik van THz vrijwel afwezig. Het THz-spectrum bleek te hoog in frequentie te zijn voor alle elektronica (uitgezonderd de meest geavanceerde en dure III-V-technologieën), terwijl het opwekken van de grote vereiste golflengte alleen mogelijk was met cryogeengekoelde quantum-cascade lasers. Door dit gebrek aan signaalgeneratoren en ontvangers ontstond de beruchte 'THz-kloof'.

In de afgelopen tien jaar heeft de vooruitgang van het CMOS-proces transistoren opgeleverd die kunnen werken op mm-golf frequenties. Hoewel CMOS transistoren geen fundamentele oscillatie en versterking ondersteunen bij THz frequenties door de beperkingen van f_{max}, kan het gebruik van harmonischen dit schijnbaar fundamentele obstakel omzeilen.

In dit werk presenteren wij onze onderzoeksresultaten naar het ontwerp en fabriceren van volledig geintegreerde THz CMOS elektronica met on-chip antennes. Door gebruik te maken van onder-f_{max} signalen om boven-f_{max} harmonischen te genereren, is het mogelijk om signaalgeneratoren van 0.54THz tot 0.61THz te implementeren in nanometer CMOS technologieën. Fundamentele oscillatoren worden gebruikt om niet-lineaire, derde harmonischen-genererende versterkers aan te sturen die vervolgens verbonden zijn met probe pads of on-chip antennes. Door nuttig gebruik te maken van parasitaire effecten en uitgebreide EM- en transistormodelering, is het mogelijk om state-of-the-art frequentie, bandbreedte en chip oppervlakte te realiseren.

De integratie van diverse on-chip antennes (dipole, gevouwen dipole, collinaire dipole array) samen met de signaalbronnen resulteert in THz stralers geschikt voor sensor arrays met hoge zenderdensiteit. Diverse beeldvormende metingen worden gepresenteerd die gebruik maken van de vervaardigde THz signaalgeneratoren. Deze tonen de haalbaarheid van THz CMOS aan voor dielektrische contrastbeeldvorming. Van deze beeldvormingsexperimenten zijn een niet-destructieve, contactloze waterinhouddetector en de verificatie van verpakte chirurgische naalden belangrijke toepassingen met echt industrieel potentieel.

Diepgaande analyses van de hoge frequentie prestaties van zowel transistoren en passieve componenten in CMOS zijn uitgevoerd en gerapporteerd. Een voorlopige studie over de compatibiliteit en impact van verschillende antenntypes en verpakkingsmethoden voor THz-elektronica wordt gegeven, naast een overzicht van actuele state-of-the-art circuits en applicaties die baat kunnen hebben bij een goedkope, massaproduceerbare implementatie in CMOS.

Injection-locked delers, superregeneratieve ontvangers (SRR) en Schottky barrier diode (SBD) detectoren zijn onderzocht als potentiële THz ontvanger circuits. Een 0.58THz SRR met flipchip dipole antenne in 28nm CMOS is geïmplementeerd, evenals SBD's met on-chip bowtie antennes voor breedbandige 0.5THz-1THz detectie. Een 30THz on-chip bowtie antenne is ontworpen met het oog op het lang-infrarood spectrum voor thermische beeldtoepassingen.

Table of Contents

List of Symbols and Abbreviations

List of symbols

α	Attenuation constant
β	Phase constant
δ	Skin depth
ε_r	Relative permittivity or dielectric constant
η_{rad}	Radiation efficiency
λ	The wavelength of a signal
λ_0	The wavelength of a signal in vacuum
μ	Permeability
ω	$2 \cdot \pi f \sim$ frequency
σ	Conductivity
υ	Wave velocity
$D(\theta, \phi)$	Antenna Directivity
f_{max}	Maximum frequency of oscillation/power gain
f_t	Cut-off or transition frequency
f_{gm}	Maximum frequency where a cross-coupled transistor pair can generate a negative resistance
G_R	Antenna gain on the receiver side
G_T	Antenna gain on the transmitter side
$G(\theta, \phi)$	Antenna Gain
HD_N	Harmonic Distortion, N-th harmonic
j	The imaginary unit
P_a	Accepted power
P_r	Radiated power
$R_\square$	Sheet resistance
$U(\theta, \phi)$	Radiation intensity
Z_0	Characteristic impedance
A	Ampere
C	Capacitance
c	Speed of light
d	Distance
D	Peak antenna Directivity

dB	Decibels
dBi	Decibels-Isotropic
f	Frequency
G	Peak antenna Gain
Hz	Hertz
L	Inductance
Mx	Referring to transistor x of a circuit
Q	Quality Factor
R	Resistance
tanδ	Loss tangent
V	Volt
W	Watt
X	Reactance
Z	Impedance

List of abbreviations

a.u.	Arbitrary unit
A-MOS varactor	Accumulation-mode MOS varactor
ABS	Acrylonitrile Butadiene Styrene
AC	Alternating Current
BW	Bandwidth
CMOS	Complimentary Metal-Oxide-Semiconductor
CW	Continuous Wave
DC	Direct Current
DCO	Digitally-Controlled Oscillator
DFM	Design For Manufacturability
DSP	Digital Signal Processing
EIRP	Equivalent Isotropically Radiated Power
EM	ElectroMagnetic
ESA	European Space Agency
FIB	Focused-Ion Beam
FSPL	Free-Space Path Loss
Gbps	Giga-bit per second
GHz	GigaHertz
GSG	Ground-Signal-Ground
HBT	Heterojunction Bipolar Transistor
HD	Harmonic Distortion
HDPE	High-Density PolyEthylene
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit

IF	Intermediate Frequency
IM	InterModulation
IO	Input/Output
IoT	Internet of Things
IR	Infra-Red
ITRS	International Technology Road-map for Semiconductors
KHz	KiloHertz
LNA	Low-Noise Amplifier
LO	Local Oscillator
MAG	Maximum Available Gain
MHz	MegaHertz
MIM-cap	Metal-Insulator-Metal capacitor
mm-wave	Millimeter-wave
MOM-cap	Metal-Oxide-Metal capacitor
MOS-cap	Metal-Oxide-Silicon capacitor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NEP	Noise-Equivalent Power
NRGC	Negative Resistance Generator Circuit
PA	Power Amplifier
PCB	Printed Circuit Board
PLA	PolyLactic Acid
PP	PolyPropylene
PS	PolyStyrene
PSG-SBD	Poly-Silicon Gate Schottky Barrier Diode
PTFE	Polytetrafluoroethylene, aka Teflon
QCL	Quantum-Cascade Laser
RF	Radio Frequency
Rx	Receiver
SBD	Schottky Barrier Diode
SEM	Scanning-Electron Microscope
SNR	Signal-to-Noise Ratio
SOI	Silicon-On-Insulator
SRF	Self-Resonance Frequency
SRO	Super-Regenerative Oscillator
SRR	Super-Regenerative Receiver
SWTL	Slow-Wave Transmission Line
Tbps	Tera-bit per second
THz	TeraHertz
TIA	Trans-Impedance Amplifier
Tx	Transmitter
UTM	Ultra-Thick Metal
VCO	Voltage-Controlled Oscillator

Chapter 1

Introduction to THz

1.1 Sub-millimeter waves in the electromagnetic spectrum

In the frequency spectrum, the terahertz (THz) spectrum ranges from 300GHz to 3THz and is located between the millimeter wave (mm wave) spectrum and the far-field infrared spectrum (Figure 1.1). Since the wavelength λ in vacuum at this frequency is shorter than a millimeter (λ_0 at 300GHz = 1mm), this frequency range can also be denominated as the sub-millimeter wave spectrum (sub-mm wave). The THz spectrum is usually seen as being on the border between electronics and optics, and the THz waves share properties from both, such as (some) transparency and the ability to do spectroscopy, just like X-ray radiation. However, in contrast to X-ray waves, THz waves do not contain ionizing energy levels and as such do not cause damage to DNA, allowing safe exposure of THz waves.

Even with the many interesting properties of the THz spectrum, the usage of THz remains limited. This is due to the lack of available THz source and detector solutions: the THz spectrum is too high in frequency for electronic components, and too low in frequency (or too high in wavelength) for optical systems. For electrical systems, the available output power of transmitters reduces with increasing frequency. For optical systems, the available output power reduces with decreasing frequency. The frequency range where both fields fail to generate enough power is the THz range, resulting in the "THz power gap". Consequently, THz systems to be used outside of well-controlled lab environments are rare, bulky and expensive. When comparing the number of consumer applications and the usage of frequencies on the spectrum (Figure 1.2), the THz gap is clearly visible as well.

Increasing research efforts over the past decades in both electronics and photonics have greatly advanced the development of the THz equipment. New applications and uses for THz waves are constantly being developed and tested, providing additional motivation and inspiration for further improvement of the THz field. To truly fill up the THz gap, compact and affordable THz sources and detectors are needed. While this

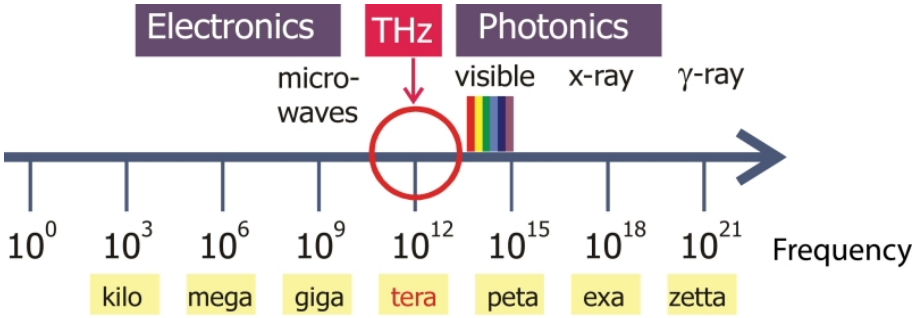


Figure 1.1: The electromagnetic spectrum, with the THz region located between the electrical en optical domain [Del16]

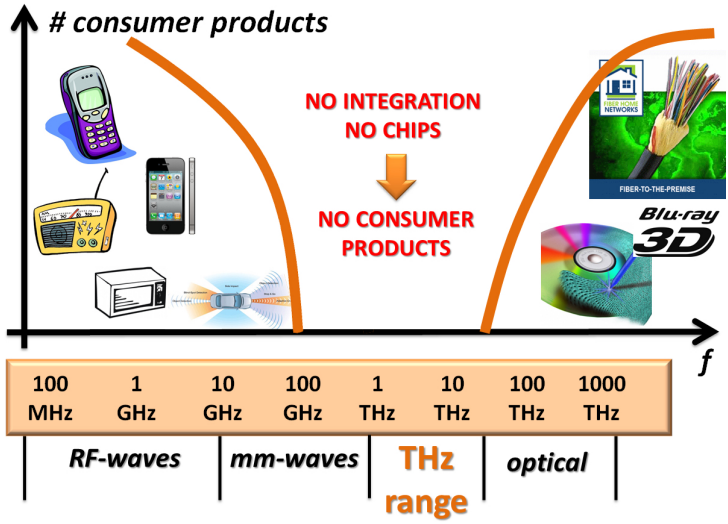


Figure 1.2: Consumer applications for different parts of the frequency spectrum, illustrating the THz gap which exists due to the limited THz source and detector solutions

seemed as a insurmountable task some decades ago, and there is still a long way to go, the outlook on the THz future is looking brighter every year.

1.2 THz applications

Even though the efforts required to fill up the THz gap can be very high, the possible applications in the THz spectrum justify the effort. A plethora of new, exciting applications become possible thanks to the use of THz waves, of which a small selection will be shortly described in the following sections. New, innovative uses of the THz waves keep emerging as the research moves forward, and will continue to amaze with the introduction of more powerful, more reliable and more affordable THz electronics and systems.

1.2.1 High-Speed data communication

The first application that comes to mind when talking about an increase in operation frequency, is high data-rate communication. According to the Shannon-Hartley theorem [Sha48], the theoretical upper bound of the data rate or channel capacity C of a certain communication channel is determined by the signal-to-noise ratio (SNR) and the bandwidth (BW).

$$C = B \cdot log_2(1 + SNR) \tag{1.1}$$

From Equation 1.1, the maximum data rate for a fixed SNR can be increased by utilizing a larger bandwidth. The available frequency bands in the radio-frequency (RF) and millimeter-wave (mm-wave) spectrum are getting more and more crowded, and large, unassigned stretches of bandwidth are no longer available at these frequencies. The THz spectrum, on the other hand, is currently unrestricted and has hundreds of GHz bandwidth available, which would allow Tbps communication links. Unfortunately, the high Free-Space Path Loss (FSPL) will pose a limit on the effective operation range of these communication links. As a result, THz communication links seem well suited for high-speed, medium to low distance communication links, both wireless and wired [Son11].

Is there, however, a need for such high data rates? One of the main drivers for high-speed data communication is the constant demand for better, higher resolution video and multimedia. According to Edholm's law of bandwidth (Figure 1.3), the data rate in the three main categories of communication links (wireline, nomadic/WLAN and mobile/cellular) increases exponentially by doubling every 18 months [Che04]. This continuing advancement allows the transition of an application from the wireline category through nomadic to the wireless domain. For example, an internet connection was originally confined to an ethernet cable (wireline). Improvement in telecommunications resulted in Wi-Fi/WLAN, which provided a limited, wireless internet connection in a local area (nomadic), before the introduction of 2G/3G enabled

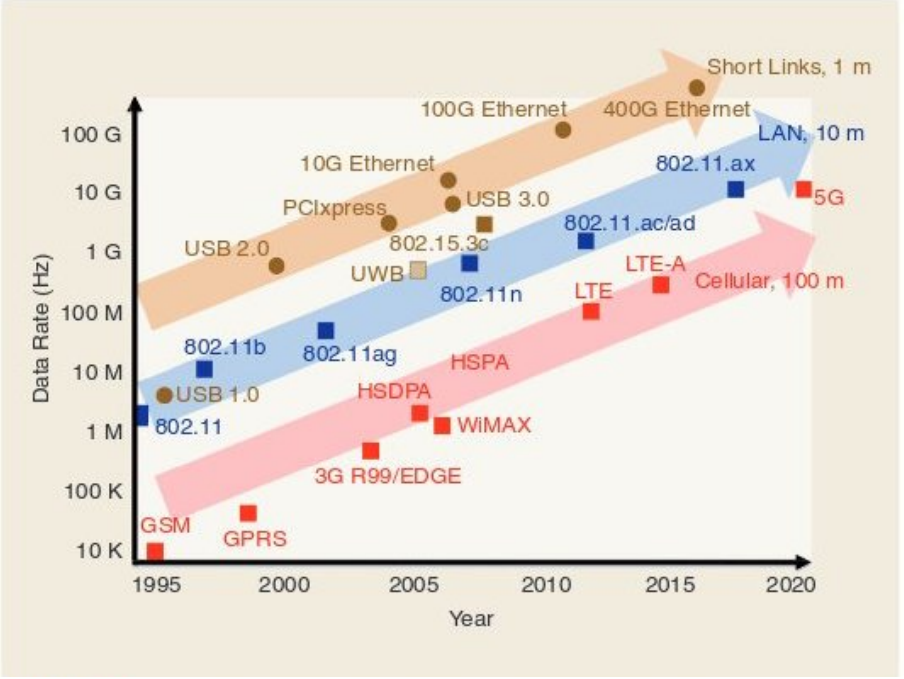


Figure 1.3: Edholm's law of bandwidth, illustrating the increasing demand for higher data rates [Dal17]

a truly mobile, wireless connection (wireless). While the three domains increase the data rate in lock-step, with the maximum data rate decreasing from wireline to wireless, extrapolations predict a convergence of the data rates of nomadic and wireless domains around the year 2030. This can be explained as these two domains strongly depend on advancement of the same RF semiconductor technology. Using Edholm's law of bandwidth, it can also be predicted that the data requirements for short-ranged wireless communication systems will exceed 10 Gb/s. This would call for an increase in carrier frequency beyond 100 GHz to obtain the necessary bandwidth [Fed10].

One of the technical showcases of the 2020 olympic games in Tokyo, Japan, will be to record and broadcast the sport events in the new 8K or Ultra-High Definition TV (UHDTV) resolution, with a 7680×4320 pixel resolution, 16 times the number of pixels of the Full HD resolution. To stream these high-data rate videos on mobile devices, a short-distance communication link should be established that can handle these very high data rates. To this effect, successful tests have been conducted with compact transceiver chips in the 300 GHz band, with data rates of up to 20Gb/s [Son16] in

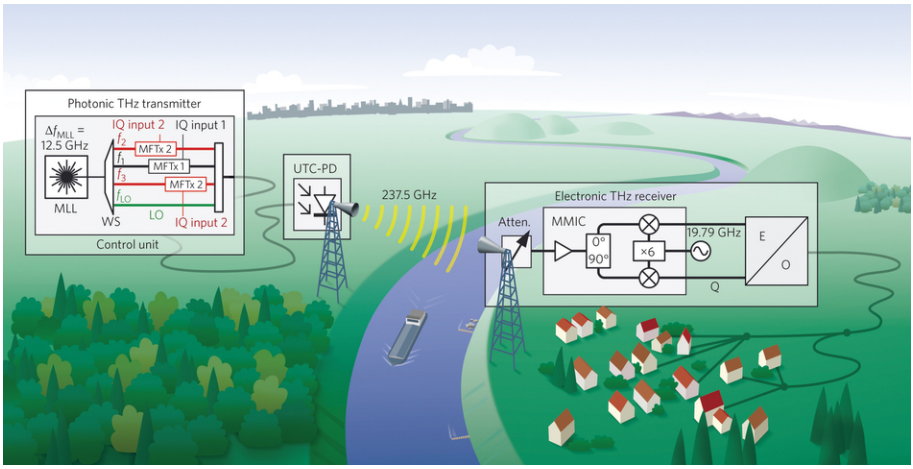


Figure 1.4: High data rate point-to-point backhaul communication using THz waves [Koe13]

a kiosk-style setup: the kiosk or data terminal is able to transfer large data files in a matter of seconds to any (mobile) device in the vicinity.

If larger antennas are possible, the limitations of the FSPL and atmospherical attenuation on the link budget will be reduced and longer distances can be covered. While these types of antennas are impractical for a consumer product, the size poses no constraint when considering point-to-point communication such as is the case for base stations (Figure 1.4). With this application in mind, data rates of up to 100Gbps have been measured over distances of 20 meters, and both the speed and distance are expected to improve [Koe13].

Another field of communication is bound to reap the benefits of the advancements in THz electronics: the short-range chip-to-chip communication. These communication links often require a very high data rate over a short distance (several centimeters), for example in the servers used in data centers. This type of communication is currently dominated by optical fiber communication. While optical fiber is excellent for long-distance communication links due to its very low attenuation of the transmitted light signals, this solution proves to be very expensive and power-consuming for the short-distance applications mentioned earlier. A wireless chip-to-chip link using on-chip antennas and THz waves, or THz waves being launched into a dielectric waveguide (Figure 1.5, [Hol17]), could facilitate the implementation of high data rate communication links at a lower cost than optical fibers.

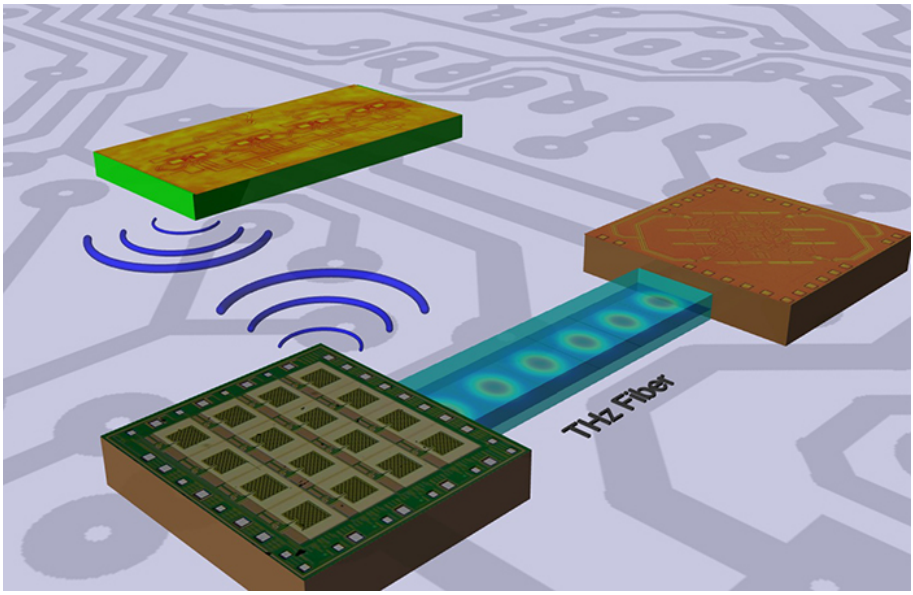


Figure 1.5: Chip-to-chip communication, both wireless and wireline, could effectively use the large available bandwidth at THz frequencies for high-speed, short distance connections [Han14]

1.2.2 Imaging

Besides communication, the (partial) transparency of materials to THz waves opens up the possibility of imaging applications. While there are many possible applications for imaging [Fri11], some main fields of interest will be highlighted.

Security and stand-off personnel screening

One of the first imaging applications being developed is the use of passive or active THz imaging for security screenings. While metal detectors can detect the presence of metallic objects, it does not detect the shape of this metal object or other non-metallic objects. In an airport security situation, this translates to a metal detector detecting non-dangerous objects such as keys, but ignoring prohibited non-metallic objects such as ceramic knives. While X-ray radiation could easily detect objects of different materials and their respective shape, the ionizing energy of the X-ray radiation makes it highly unsuited for use on humans. Additionally, the generation of X-rays require a

Figure 1.6: Stand-off personnel scanning using THz radiation, showing a hidden knife held by the person being screened [App07]

gyrotron, a costly and non-compact device. Because of the high demand for accurate, contact-less (stand-off) personnel screening, mm-wave and THz radiation systems are intensively being developed. These security systems can detect hidden objects (metallic and otherwise) and shapes without endangering the health of the passengers being screened, as depicted in Figure 1.6. The range for these systems can go up to several meters, which also provides a safe distance between the system operator and a potential threat.

Medical imaging

The THz imaging capabilities are also being developed for more peaceful applications, such as health care. Cancer, tumors and malignant tissue matter detection can be done using THz waves [sY16]: the absorption and reflection of THz waves depends on the chemical composition of the tissue being scanned. Since tumor cells are different from healthy cells, they will absorb and reflect THz waves differently (Figure 1.7). By measuring the reflection and absorption rate of the tissue being scanned, and comparing it with other (known) reference results, tumor cells can be detected using THz imaging. The exploitation of this variation in THz response could lead to several useful medical imaging devices. Rapid-scanning, low-cost skin cancer detectors could find a large user base with dermatologists and people with an increased risk of melanoma. The THz imager could quickly determine if a mole or other skin feature is benign or malignant without the need of a biopsy. A more specialized application would be a rapid response analysis tool to perform a fast diagnose of tissue before, during and after tumor or cancer removal surgery, providing immediate feedback to the surgeon. In a similar

fashion, the healing process of skin burn patients can be monitored without having to remove the bandages, as the THz waves can easily penetrate through the gauze [Tay11].

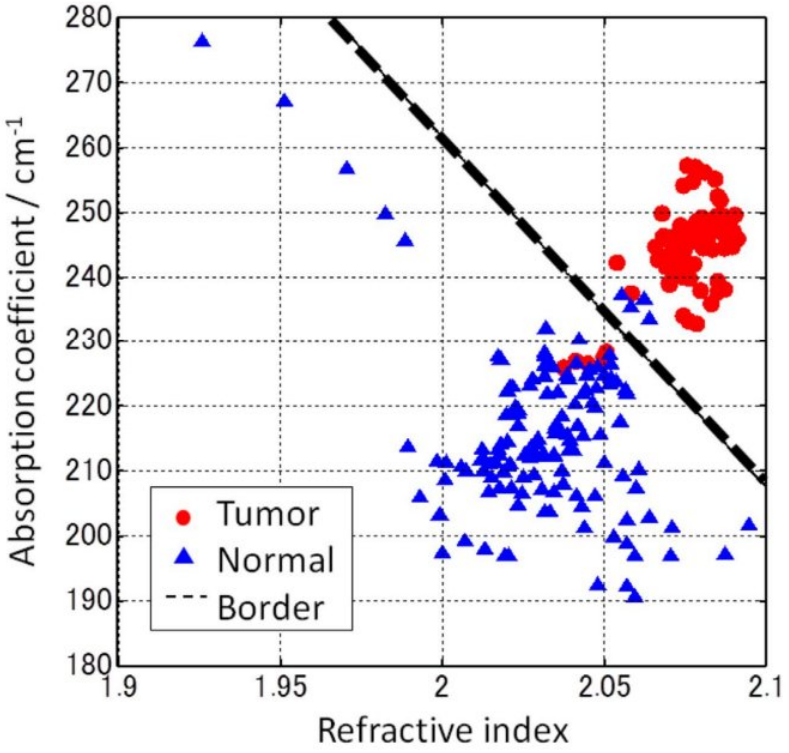


Figure 1.7: Differences in absoprtion and refractive index of tumor and healthy brain cells from rats under THz radiation. [sY16].

Another interesting field of application is dentistry: while visual inspection of cavities on the top side of teeth is done by the dentist, proximal surface carries between teeth can occur and are very difficult to detect using visual inspection (Figure 1.8). Therefore, an X-ray radiography is necessary to detect these carries. The implementation of THz detection tools, which are non-ionizing, would allow a more frequent examination of potential proximal surface carries without increasing the exposure of both patient and dentist to harmful ionizing radiation. Further analysis and screening of the internal composition of teeth can also be done with a minimal effort or need of complex and invasive methods. The THz imaging device can even be implemented in a compact form factor to enable easy maneuvering in the tight confinements of the human mouth.

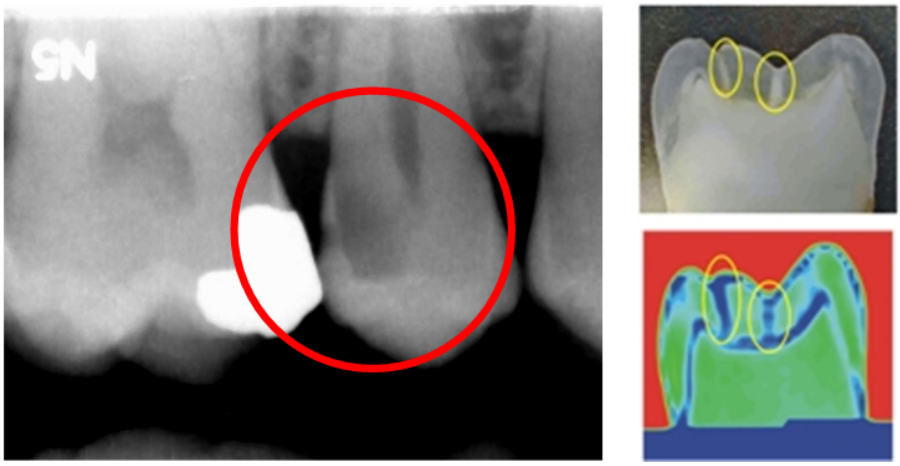


Figure 1.8: X-ray image of hard to detect proximal carries (left), and a comparison between an X-ray (top right) and THz image of a tooth with two marked top carries (bottom right) [Ter16].

Archeology and art conservation

When looking at an object, the viewer uses the visible light to create an image of the object. However, when researchers, historians and conservation experts are analyzing an ancient painting or object, they are not only interested in the top, visible layer of the painting. The supporting structure of the painting or hidden paint layers below the top layer are all part of the history of the art piece. When analyzing these hidden parts of a painting, different parts of the spectrum are used as shown in Figure 1.9. As radiation from different parts of the spectrum can penetrate different types of materials, each gives another viewpoint of the object being scanned. The advantages of THz radiation for subsurface imaging in the Archeology and Art field is its deeper penetration in the material than infrared, portability and safety compared to X-ray and its sensitivity to water and humidity thanks to the collective excitation of water molecules by THz radiation [Jac11]. Moderate radiation with THz waves does not heat up or damage the sample, which is a crucial requirement when working with unique, ancient and fragile test subjects.

Ancient books and manuscripts provide an additional challenge for historians, as some are so fragile or in an advanced state of decomposition that the mere act of opening them would cause irreparable damage. Recently, it has been demonstrated that by illuminating a stack of papers with THz waves and measuring the reflected waves, it is possible to reconstruct the text written on each individual page without touching or

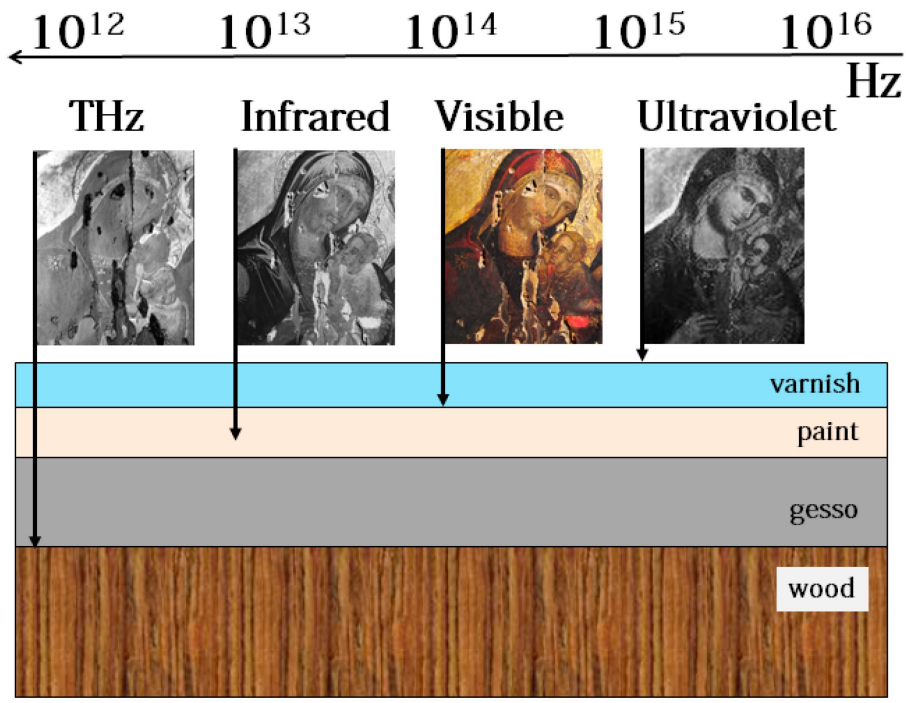


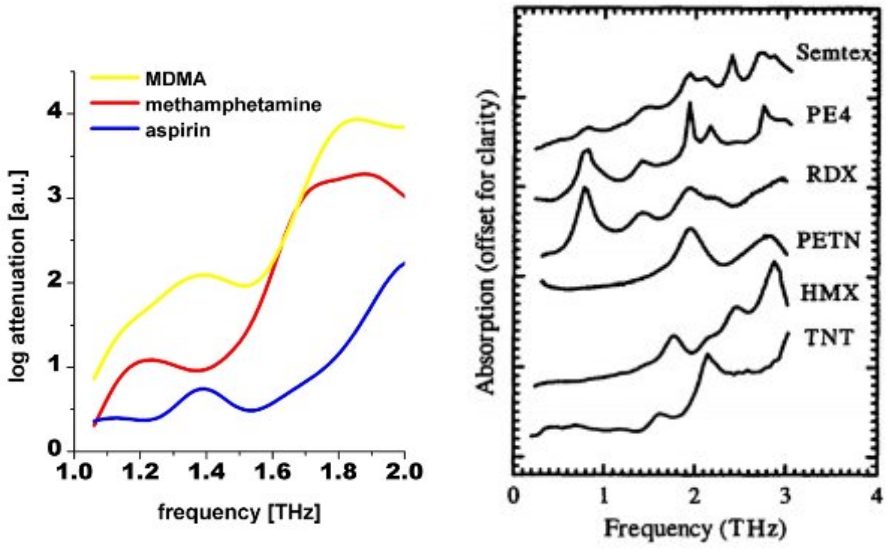
Figure 1.9: Different parts of the spectrum can penetrate different types of material [Cos16]

manipulating the pages [RS16]. While there are still many improvements to be made on both penetration depth, accuracy and speed, this shows that THz research is able to provide unexpected solutions to some long-standing archeology problems.

1.2.3 Spectroscopy

Depending on the material being scanned, the reflected, absorbed and transmitted THz signal can drastically vary. As a result, the broadband frequency response of a THz pulse generates material fingerprints which can be used to distinguish the material of objects being scanned. This act is called 'spectroscopy' and could prove very helpful when trying to identify materials that look similar, such as white powders or tablets, or to detect very small concentrations of a material or chemical substance (Figure 1.10).

The possible applications vary from extending the spectroscopy range from the IR



(a) (b)

Figure 1.10: Spectroscopy examples showing the different spectral fingerprints of drugs (a) [Kaw03] and explosives (b) [Fed05]

region to the THz region for detailed analysis in laboratories, to compact hand-held devices. A whole host of different use cases can be proposed that can benefit from the spectroscopy applications of the THz spectrum, such as narcotics detection when scanning packages, augmented security screenings by detecting trace amounts of explosives, fast identification of medicine to prevent wrongful administration, as well as analyzing the purity and consistency of motor oils without the need of sending samples to the lab.

1.2.4 Quality Control

Interest in the THz spectrum is also increasing from production and industrial partners due to the (semi-)transparent behaviour of THz signals with different materials. The non-destructive testing (NDT) of (partially-)finished parts and products is an important aspect of quality control (QC) of the production process. In mass-production lines, the rapid detection of process deviation and anomalies allows for a good control of the process and minimizes costly post-production alterations, recalls and inferior products. While NDT and QC systems already utilize X-ray and visible light solutions, they each

have limitations and trade-offs in terms of resolution, speed, safety and compatibility with different materials and environments. Table 1.2.4 shows the comparison for the case of NDT in the wood processing industry, where transparency, resolution, safety and the ability to detect fibre structures are the dominant performance indicators. The usage of THz signals in a NDT context adds a new alternative to these existing methods with another balance between the different performance parameters.

Method	Transparancy	Resolution	Safety	Detect Fibres	Cost
X-Ray	✓	✓	-	-	High
Visible	-	✓	✓	✓	Low
Infrared	-	✓	✓	✓	Medium
Terahertz	✓	✓	✓	✓	Low
Microwave	✓	-	✓	✓	Low

Table 1.1: Table comparing different NDT methods across the frequency spectrum for the wood industry [Bas16]

Compared to X-ray, the main advantage of THz is the non-ionising energy of the radiated waves, which means that THz radiation is harmless for biological tissue. Unlike X-ray, this makes the use of THz radiation safe in environments where contact with humans or other living beings is possible.

The transparency property of the THz spectrum also allows testing of opaque materials such as colored plastics and polymer materials. Visible light imaging and cameras used in NDT are often limited by the optical transparency of the material, and may for example not adequately image colored or dark materials.

1.2.5 Space exploration

In the continuing quest to explore and learn about the universe, space agencies and research centers look to space not only using visible light telescopes, but increasingly with detectors for other parts of the frequency spectrum. This multi-spectral approach has yielded a trove of information and has deepened our understanding of the origins of the universe and the formation of stars. Besides IR, X-ray and other high-energy radiation waves, the THz spectrum is also gaining importance as an astronomy tool. The Herschel space mission from the European Space Agency (ESA) for example, measured radiation in the THz and far-field IR spectrum from different star systems [Pil10]. This provided an additional layer of information that can be combined with the X-ray and visible light imaging. One of the very useful applications of THz astronomy is the analysis of gas clouds and nebulas (Figure 1.11) thanks to the spectral fingerprints of different chemicals in the THz spectrum.

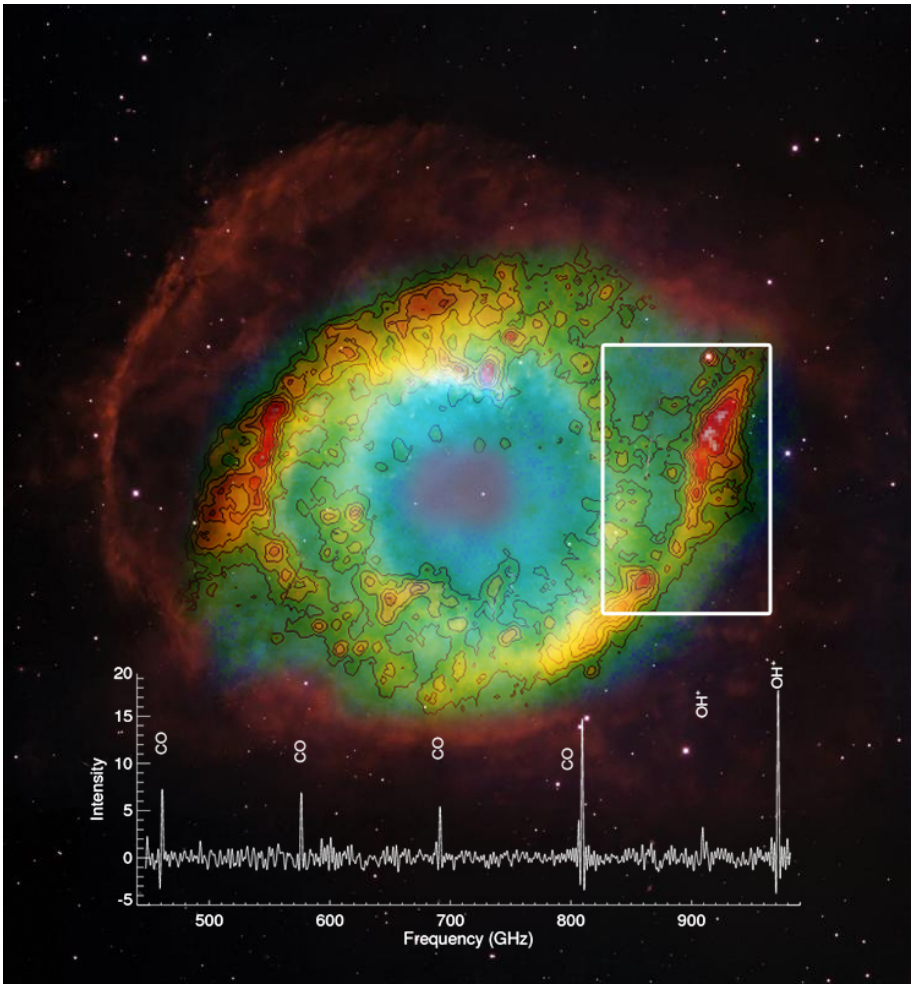


Figure 1.11: Spectral fingerprints indicating the presence of CO and OH^+ molecular ions in the Helix Nebula (NGC 7293, also known as the 'Eye of God"), an essential component in the formation of water, during the ESA Herschel mission [Etx14]

1.3 Why CMOS

Efforts to bridge the THz gap are being undertaken, in both electronics as optics. The electronic field works on increasing the operation frequency and output power, while the optics field aims at reducing the operating frequency of current optical source solutions. A very brief overview of some of the issues for both approaches will be given in the following section. As this work focuses entirely on CMOS electronics, some more in-depth analysis will be provided in the following chapter.

1.3.1 Optics

While electronics keeps increasing their operating frequency, there is a parallel effort to reduce the operating frequency of optical devices. Photomixing, an optical technique used in the the IR and higher spectra, can be used to downconvert shorter-wavelength signals to generate THz signals. One of the most promising paths for optical THz generators are the Quantum-Cascade Lasers (QCL), which can be thought of as long-wavelength lasers. Using QCL, high output powers over hundred mW in CW mode [Wil06] and a record 1W in pulsed mode [Deu14] have been demonstrated in the THz frequency range. However, the main practical roadblock for the widespread use of QCL devices is that they are not room temperature stable: QCLs require a very low operational temperature (Figure 1.12) and thus extensive cooling, which impedes its use in widespread, portable and affordable consumer applications.

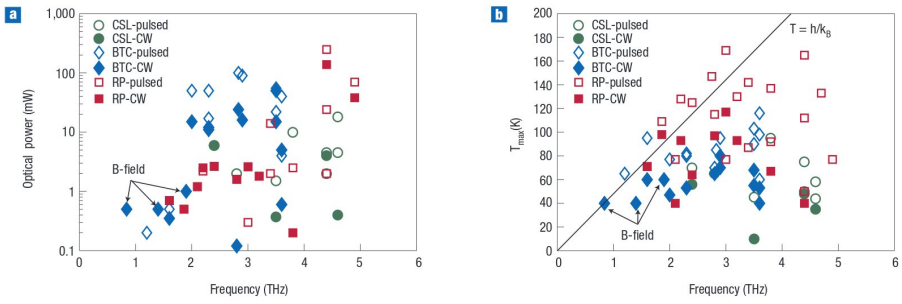


Figure 1.12: Plots showing the peak output power QCL THz sources, and the corresponding maximum operating temperature [Wil07]

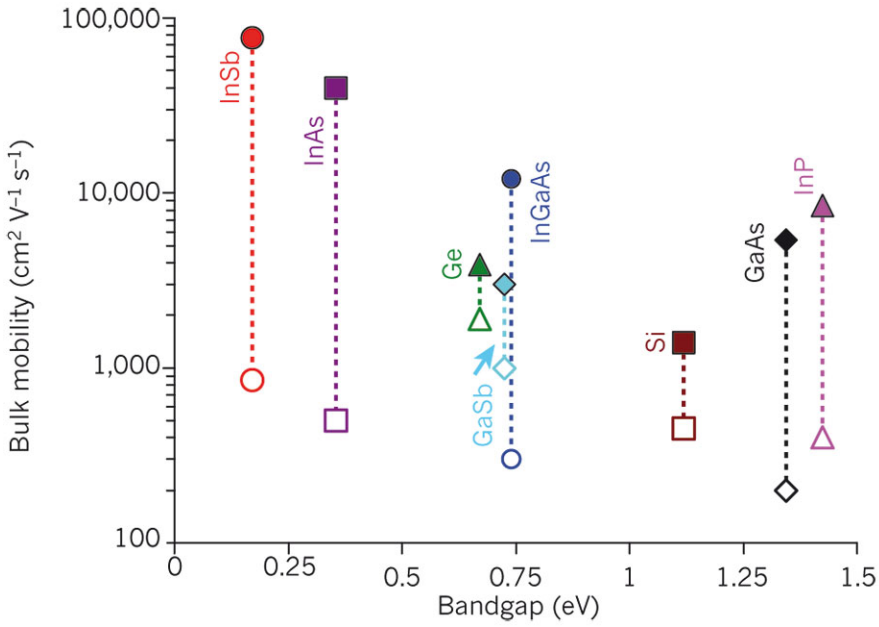


Figure 1.13: Mobility for different types of semiconductor materials [Pil11]

1.3.2 Electronics

III-V

The III-V technologies have always been at the forefront of high-frequency electronics. Due to their high mobility (Figure 1.13), technologies such as InP, and InGaAs can reach much higher fundamental operation frequencies than the silicon-based technologies [Cha11] [Sam11]. The f_{max} of these process techniques have already crossed the 1THz milestone [Lai07], and the first monolithic integrated electronic circuit to operate above 1THz was demonstrated in 2015 [Mei15] and used a 25nm InP High-Electron Mobility Transistor (HEMT) process to achieve a 9db, 9-stage amplifier at 1.03THz. Unfortunately, the fabrication of electronic circuits in these III-V technologies is very expensive, not suited for large volumes and not integratable with digital circuits for signal processing. Therefore, the usage of III-V technologies remains limited to low volume, high-cost and high-performance niche markets such as space, defense, medical and highly specialized industrial applications.

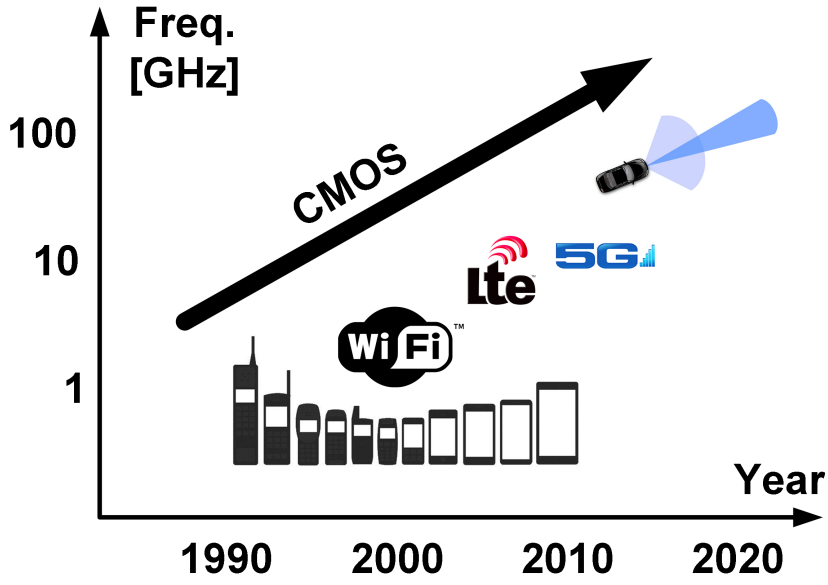


Figure 1.14: Increase of frequency over the years for consumer products due to the advancements of high-frequency CMOS performance

Silicon technologies: CMOS and SiGe

Silicon-based technologies have a lower mobility than the earlier-mentioned III-V technologies, but are considerably cheaper and easier to produce, and in much larger quantities.

Thanks to the advancements of CMOS technology in the last 50 years following Moore's law [Moo65], the frequencies that can be generated and detected by CMOS circuits keeps on increasing. Combined with the increase in digital circuit density and cost reduction due to scaling, this enables a widespread usage of consumer products utilizing these frequencies (Figure 1.14). In addition, the number of RF CMOS transceivers in one product keeps increasing (cellular, Bluetooth, WiFi,...). A prime example of the market-disrupting power of CMOS is the mobile revolution that started around 1990 with the emergence of RF CMOS circuits. Nowadays, the CMOS process has advanced to the point where THz circuits can be fabricated and can start to compete with III-V. While CMOS is the most challenging semiconductor technology to generate THz signals, the potential benefits clearly reward the effort: full integration with digital circuits, low-cost production and available infrastructure to mass-produce millions of units per week would allow the implementation of THz sources and detectors in

consumer products and impact the daily life of people everywhere.

However, there are some serious roadblocks for THz CMOS circuits: the low breakdown and supply voltage, the low fmax limiting fundamental high-frequency operation, and the lossy silicon substrate. While SiGe performs better for fmax and breakdown/supply voltage, silicon technologies lack the THz performance of the III-V technologies. As a consequence, non-linear circuit techniques and a different design approach should be taken compared to III-V technologies when implementing THz circuits in silicon technologies.

1.4 Thesis overview

In the previous sections, the usefulness of the THz spectrum was clearly demonstrated along with a brief overview of the main contenders to fill the THz gap.

The aim of this work is to investigate the possibilities of THz integrated circuits in CMOS technology: both on a circuit design level and the applications of the fabricated circuits. While CMOS is the most challenging technology for THz electronics, it also has the potential to have the largest impact on consumers and markets where low-cost, compact circuits with full integration with digital signal processing (DSP) circuits is required: the THz imaging array and read-out circuit, analog-to-digital conversion and image processing functionality (feature extraction, image recognition) can all be combined in one CMOS chip. The results of this work are also of interest for specialized, niche markets with low product volumes that utilize other process technologies. Design techniques and methodologies that will be demonstrated in CMOS can successfully be applied in III-V or SiGe technologies as well. This will result in increased performance thanks to the higher mobility, higher supply voltage and better semiconductor substrates, as well as further extend the frequency range that can be covered by electronics: a design technique for tripling the frequency of a 200GHz CMOS VCO can be used as a basis for tripling a 500GHz InP circuit to 1.5THz.

The structure of this work is as follows:

- Chapter 2 discusses the different components and building blocks that will be used to design the THz integrated circuits. Different performance metrics of both active and passive components available in the CMOS process will be presented, as well as their limitations and design trade-offs in the THz frequency range.
- Due to the tremendously high frequency of operation, getting the THz signals on and off the chip is becoming increasingly difficult. In Chapter 3, the possibilities of on-chip antennas will be discussed, as well as some of the problems of common IO methods at THz frequencies.

- In Chapter 4, the knowledge of the previous chapters is applied in the design of transmitter circuits operating above 500GHz. Oscillator concepts and design choices specifically related to operating in the THz spectrum will be explained, as well as the design of several on-chip antennas to radiate the generated THz signals off-chip. The fabricated radiating transmitters are used in different imaging setups, demonstrating the feasibility of a useful THz CMOS imaging system.
- Chapter 5 will cover the design of receiver circuits designed in CMOS to detect the radiated THz waves. Important figures of merit, specifications and possible topologies will be discussed, as well as the implementation of a Super-Regenerative Reveiver (SRR) and Schottky Barrier Diode (SBD) detector.
- The final chapter of this work (Chapter 6) will provide an overview of the realized work, as well as extensive conclusions, trends and future work on the circuit, antenna and application level. As this is the first work of our research group operating in this part of the frequency spectrum, a reflection on the techniques and experiences of this work will benefit further research on the final frontier of the electromagnetic spectrum.

Useful units and definitions when talking about THz frequencies:

- Free-space wavelength λ_0 at 1THz = 333μm
- Signal period at 1THz = 1ps
- Millimeter-wave band = 30GHz-300GHz
- Sub-millimeter-wave or Terahertz band = 300GHz-3000GHz = 0.3THz-3THz
- Sub-Terahertz range = 0.1THz-1THz
- Far-Field Infra-Red (IR) = 1THz-12THz

Chapter 2

Sub-mm wave CMOS components

Designing integrated circuits in the sub-mm wave spectrum differs significantly from analog design. Assumptions and simplifications that can be made at lower frequencies become invalid at higher frequencies, the use of S-parameters to represent power waves becomes prevalent, wavelengths become so short that transmission line effects start to manifest in small sections of interconnect, ... This chapter aims to discuss the difficulties and possibilities of the available components when designing circuits for the THz spectrum. As the low-frequency models of these components are no longer valid at mm-wave and higher frequencies, more accurate equivalent models will be provided to allow insights in the behavior of these components. Both active and passive device components will be discussed, as well as some limitations and constraints in the design process that are becoming more and more dominant in modern nanometer CMOS processes.

2.1 Scaling of CMOS and the emergence of high-frequency design

The most important active component in modern day electronics is the transistor. The dominating technology for consumer electronics is CMOS thanks to the continous scaling over the past 50 years following Moore's law [Moo65], an observation/prediction by Gordon Moore, CTO of Intel, in 1965. Moore's law states that the number of transistors that can fit on the same area in an integrated circuit will double every two years (Figure 2.1). This exponential improvement has resulted in two possibilities: the ability to make the same circuit on a smaller area (cheaper), or to place more transistors on the same silicon area (increase complexity), and resulted in the ubiquitous presence of computers, laptops and mobile phones.

The main focus of the CMOS process was, and still is till this day, the improvement of digital circuits: the flagship products of industry leaders such as Intel that drive the CMOS scaling are digital processors and memory cells. Transistor scaling benefits

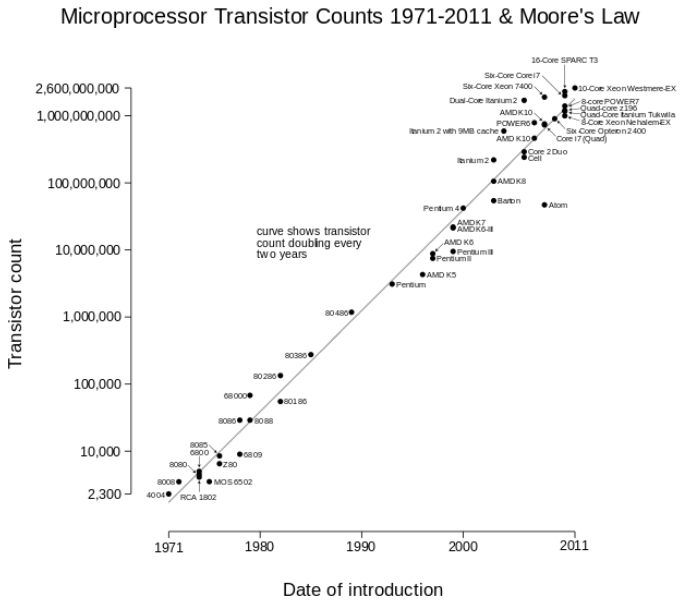


Figure 2.1: Moore's law, which predicted the doubling of the number of transistors on an IC every 2 years [Wik11]

the digital performance, but as a side effect also increases the achievable frequency of operation for analog circuits. Starting around 1990, the advancement in analog CMOS performance had improved sufficiently to lead to the development of RF CMOS circuits, which started to challenge the then-dominant III-V and Ge technologies in the RF/GHz spectrum range.

> "RF is a solved problem. And using an inferior technology like CMOS to solve it yet again is stupid-squared." -Unnamed MIT professor, 1986

This continuing, exponential improvement of RF circuits and the co-integration with digital circuits directly resulted in the explosive growth of the mobile phone market and the emergence of wireless, interconnected "Internet of Things" (IoT) devices and mm-wave radar applications. In a time span of 20 years, CMOS went from an unfeasible contender to the dominant RF IC technology. With the current deep-scale nanometer CMOS nodes pushing the frequency limit higher and higher, the THz frequency spectrum has come within reach of CMOS researchers (Figure 2.2). While

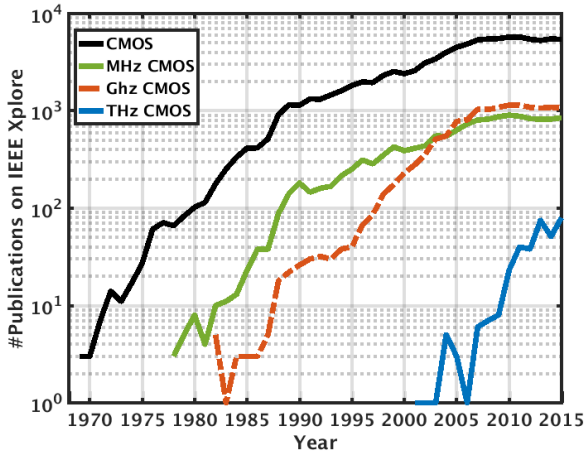


Figure 2.2: Number of publications on IEEE Xplore with the respective key words over the last 50 years, showing the emerging research interest of THz CMOS

there is still a long way to go, it seems realistic that THz CMOS is poised to experience a similar trajectory as RF CMOS.

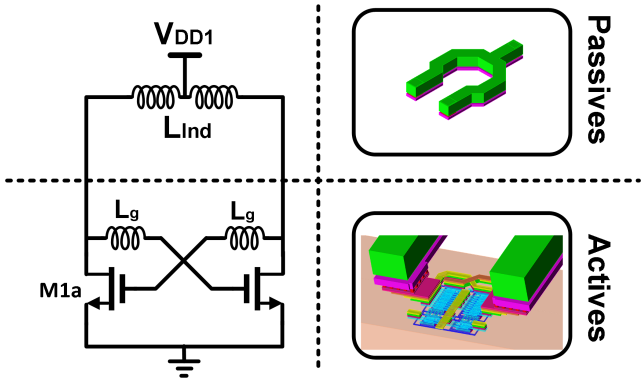


Figure 2.3: Schematic of an LC VCO in a CMOS technology, and the division between passives and actives modeling

To analyze the different components that together form a THz integrated circuit (Figure 2.3), this chapter will separately discuss CMOS transistors or 'actives' (Section 2.2) and 'passives' (Section 2.3) such as inductors, transformers and transmission lines.

2.2 Transistors at THz frequencies

Before discussing the optimal transistor size for THz frequencies, one must ask what properties make for a good high-frequency technology. High semiconductor mobility, large voltage swing, good thermal conductivity and high saturation velocity are all preferred characteristics of a THz process technology. The Johnson limit [Joh65] is a Figure-of-Merit (FoM) indicating high-frequency performance limitations, and consists of the intrinsic breakdown field E_B and saturation velocity v_{sat}. Of all the main semiconductor materials, Si and Ge perform considerably lower than InP, GaAs and InGaAs.

$$\text{Johnson FoM} = \left(\frac{E_B \cdot v_{sat}}{2 \cdot \pi}\right)^2 \tag{2.1}$$

Besides semiconductor material, there is also a difference in transistor structure. A cross-section of the three dominant transistor types at high frequencies are shown in Figure 2.4. These are the MOSFET (CMOS technology), the Heterojunction Bipolar Transistor (HBT, GaAs/InP/SiGe) and the High-Electron Mobility Transistor (HEMT, GaAs/InP/GaN). Compared with the HBT, HEMT and MOSFET have a relatively planar structure, making the transistor performance depend on the minimal horizontal feature length and advancements in lithography in contrast to the minimal vertical feature length and precise atomic growth capabilities of the HBT.

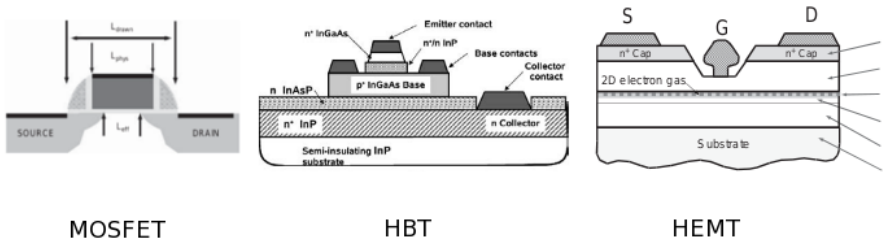


Figure 2.4: Cross-section of a CMOS transistor, HBT and HEMT [Voi13a]

Compared with other technologies, CMOS has the lowest mobility of them all, but remains the most popular and dominant technology because of its very low cost due to its mass production capabilities. Fundamental oscillation in CMOS has been

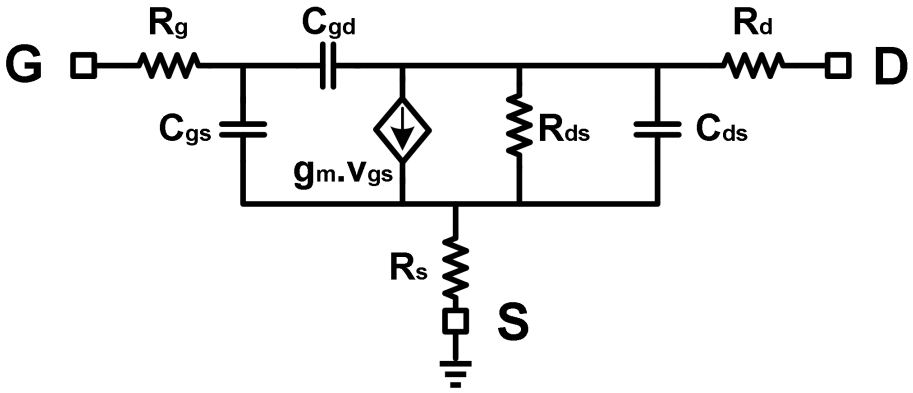


Figure 2.5: Small-signal equivalent model of the intrinsic MOSFET model with series gate, drain and source resistances

demonstrated up to 300GHz [Raz11], whereas (InP) HEMT technology reaches frequencies well above that [Sam11] and already demonstrated 1 THz amplifiers [Mei15] , but will not be implemented in consumer products due to its cost and low-volume production process.

The CMOS technology is a complementary technology, offering both NMOS and PMOS transistors. The speed of the NMOS transistor is higher than the PMOS due to the difference in carrier mobility (although this difference is diminishing with more advanced technology nodes). Since this work revolves around the highest speed achievable in the CMOS process, we will mainly focus on the behaviour and performance of the NMOS transistor.

2.2.1 CMOS transistor, f_t, f_{max}

The high-frequency potential of a transistor is often expressed using the transition frequency f_t and the maximum frequency of oscillation f_{max}. These are often used as abstract FoM to compare different process technologies, but become very real limitations when designing circuits operating in the THz band.

The transition frequency or unity current gain frequency f_t is defined as the frequency at which the current gain of a transistor becomes unity (Eq. 2.2). By shorting the drain (D) and source (S) in the small-signal equivalent model of an NMOS transistor (Figure 2.5), the current gain can be calculated and Equation 2.3 for f_t can be derived [Tas89] :

$$| H_{21}(f = f_t) | = 1, \text{ where } H_{21}(f) = \frac{I_{out}(f)}{I_{in}(f)} = \frac{Y_{21}(f)}{Y_{11}(f)} \tag{2.2}$$

$$\frac{1}{2 \cdot \pi \cdot f_t} = \frac{(C_{gs} + C_{gd})}{g_m} + \frac{(R_s + R_d) \cdot (C_{gs} + C_{gd})}{g_m \cdot R_{ds}} + C_{gd} \cdot (R_s + R_d) \tag{2.3}$$

$$\Longrightarrow f_t \approx \frac{g_m}{2 \cdot \pi \cdot (C_{gs} + C_{gd})} \tag{2.4}$$

The more commonly used expression for f_t is the simplified Equation 2.4, based on the intrinsic small-signal model excluding series resistances. While the first term on the right-hand side of Equation 2.3 strongly dominates f_t in older CMOS technologies, the impact of the other terms increase when going into deep nanometer-scale technology nodes. For a 90nm CMOS technology node, according to [Dic06], the first term $(C_{gs} + C_{gd})/g_m$ accounts for 80% of f_t while the third term $C_{gd} \cdot (R_s + R_d)$ determines 15%.

When designing and measuring high-frequency integrated circuits, power and power gain take a more prominent role than current and voltage gain. This is also echoed by the usage of S-parameters, the ratio of incident and reflected power waves, to describe transmission and reflection behavior of the device.

The maximum frequency of oscillation, f_{max}, is the frequency at which the maximum available power gain (MAG) of a transistor becomes 1, or equal to 0 when expressed in dB (Eq. 2.5). This is the highest frequency where the transistor is able to deliver gain in an ideally input/output matched scenario, and marks the frequency where the device goes from an active to a passive device. An approximated expression [Bur00] is given by Equation 2.6, and immediately shows the dependence of f_{max} on the series resistances as opposed to f_t, especially gate resistance R_g.

$$G_{max,dB}(f = f_{max}) = 0, \text{ where } G_{max}(f) = MAG(f) = \frac{P_{out}(f)}{P_{in}(f)} \tag{2.5}$$

$$f_{max} = \frac{f_t}{2 \cdot \sqrt{[g_{ds} \cdot (R_g + R_s + r_{ch}) + 2 \cdot \pi \cdot R_g \cdot C_{gd}]}} \tag{2.6}$$

While the transition frequency f_t can easily be increased by scaling down the transistor length, the f_{max} is more heavily dependent on the parasitic resistance and capacitance associated with the transistor layout, which will be discussed in Section 2.2.2. In Figure 2.6, the G_{max} of an NMOS transistor in a 40 nm technology is plotted for two different gate biasing voltages. The point where the G_{max} curve crosses 0 dB is the f_{max} point, which can differ strongly depending on the transistor biasing and layout.

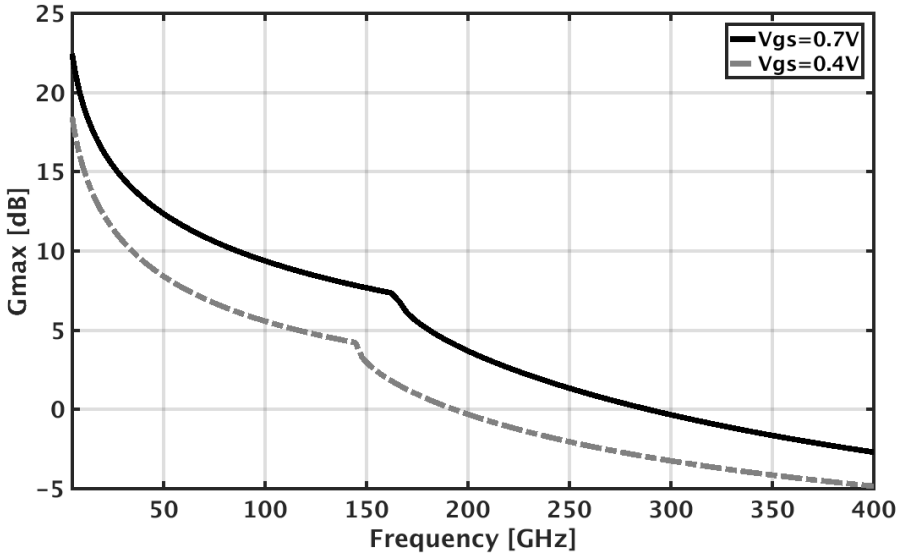


Figure 2.6: G_{max} curve of a NMOS transistor at different biasing points, showing the stability knee-point and the frequency of maximum power gain, f_{max}

As mentioned in section 2.1, CMOS is primarily a digital technology. The reduction of gate length and size following Moore's law is mainly to increase the complexity of digital circuits on the same silicon real estate, to reduce power consumption and increase processing speed up to several GHz. This scaling also has a positive effect on the RF/high-frequency performance, and as a result newer CMOS technology nodes enable circuits at higher and higher frequencies: the increase in g_m with decreasing device feature size improves the f_t and in return f_{max}. The evolution of both f_t and f_{max} is tracked and predicted by the International Technology Road-map for Semiconductors (ITRS), and the improvement with scaling is illustrated in Figure 2.7. While the predicted values of the f_t remain consistent over the years of reporting, the accuracy of the f_{max} road-map is definitely lower as reflected by the shifting values with each report. This can be attributed to an underestimation of parasitic effects in deep sub-micron technologies, with the ITRS f_{max} predictions of future technology nodes becoming more and more difficult due to the rising importance of these parasitics.

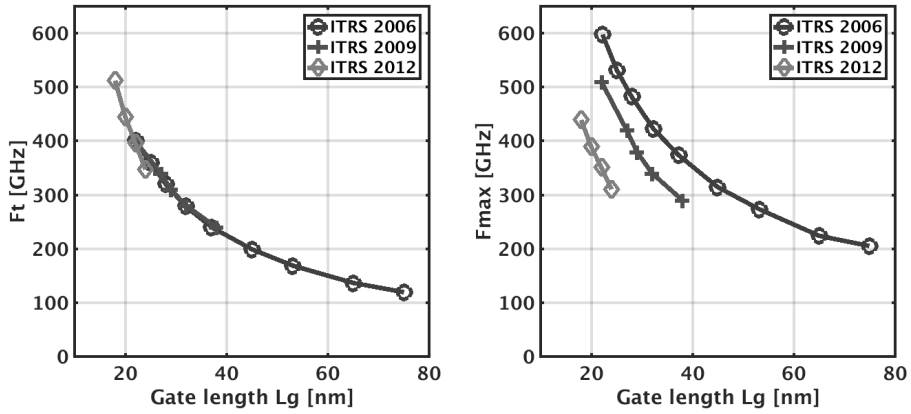


Figure 2.7: ITRS road-map of the f_t and f_{max} for decreasing transistor length [Int12]

2.2.2 Transistor layout, modeling and optimization for THz operation

When examining the high-frequency performance of transistors, the intrinsic model of the transistor no longer suffices, and the extrinsic model (Figure 2.8) including parasitic resistance, capacitance and inductance of the transistor interconnect should be evaluated. From Equation 2.6, it is concluded that the actual transistor layout will have a crucial impact on the high-frequency performance through the extrinsic parasitic resistances R_g, R_s and C_{gd}.

The source and drain resistance R_s and R_d, like most parasitic parameters in the extrinsic model, are inversely proportional to the total gate finger width W of the transistor. In addition, the number of via contacts for source and drain should be sufficiently large: the resistance of individual via contacts roughly doubles for each technology node, which can add a significant series resistance to the source and drain paths of small transistors in deep-scale nanometer CMOS.

The dominant layout component determining the high-frequency performance of a transistor is the gate resistance R_g, which is proportional to W. Since all other parasitic capacitances and resistances are inversely proportional to W, the high-frequency transistor can be optimized by adequately choosing the transistor width W_f and the corresponding number of fingers N_F. Figure 2.9 shows three different layout styles of a transistor with the same fixed length L and total width W.

The gate resistance R_g can be expressed as:

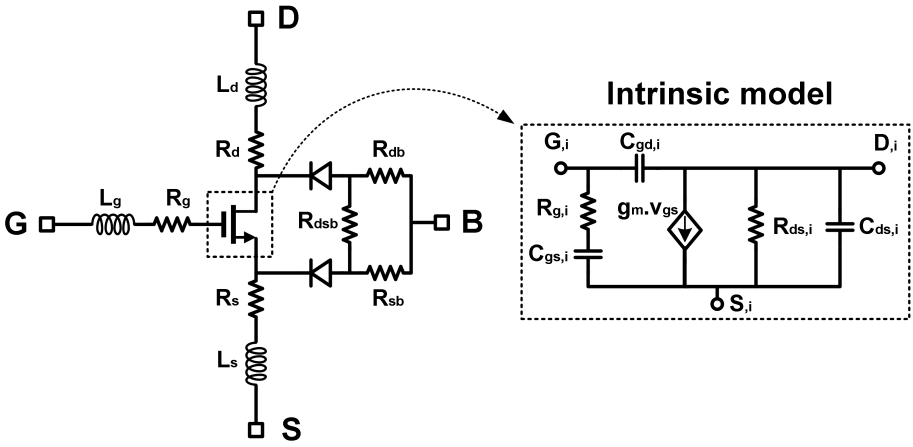


Figure 2.8: Simplified extrinsic model of a NMOS transistor including series resistance, inductance and substrate losses

$$R_g = \frac{R_{sh,gate} \cdot W}{3 \cdot n_{g,con}^2 \cdot N_F \cdot L} + \frac{R_{vert}}{N_F \cdot W \cdot L} + \frac{R_{via,gate-metal}}{n_{via,gate-metal} \cdot N_F} + \frac{R_{interconnect} \cdot N_F}{\xi \cdot n_{g,con}} \quad (2.7)$$

Where $R_{sh,gate}$ is the gate sheet resistance (different for poly or metal gates), $n_{g,con}$ the gate contact number (equal to 1 for single sided gate contacts, and equal to 2 for gate contacts on both sides), R_{vert} the gate vertical contact resistivity for the silicide-polysilicon interface [Lit01], $R_{via,gate-metal}$ the resistance of a contact via connecting the gate material with the metal routing layer, $n_{via,gate-metal}$ the number of gate-metal contact vias used per finger, and finally $R_{interconnect}$, the resistance of an interconnect segment connecting all the individual gates together and ξ an additional weight to factor in the specific distributed network effect of the chosen interconnecting layout.

For broad finger widths, the horizontal finger resistance (first term of Equation 2.7 [Raz94]) is dominant, and the total gate resistance can be reduced by implementing a larger number of narrow fingers (Figure 2.9 a and b). A further improvement to the transistor layout is by placing contacts on both sides of the gate (Figure 2.9 c): the current flowing through the gate is divided into two paths of $W_f/2$ length, effectively breaking up the intrinsic gate resistance into two resistances in parallel. This reduces the horizontal finger resistance by 4, and is included in Equation 2.7 by the $n_{g,con}$ component. By just considering the horizontal gate resistance, one could conclude that the same result as using gate contacts on both sides can be achieved by halving the individual finger width W_f and doubling the number of fingers. However, the width

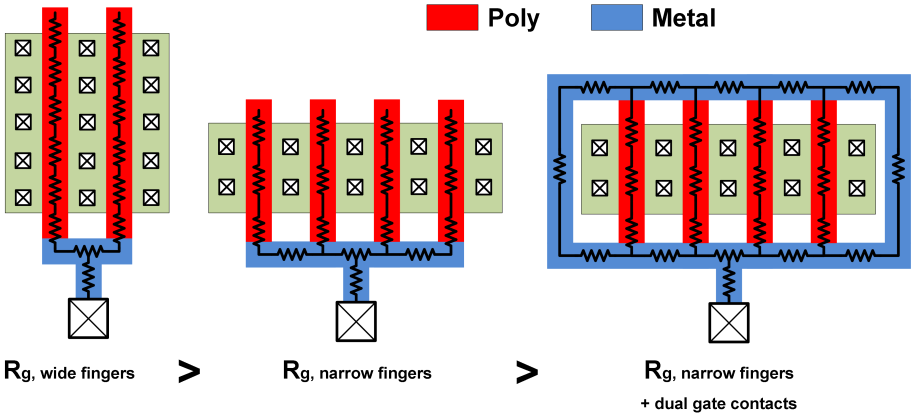
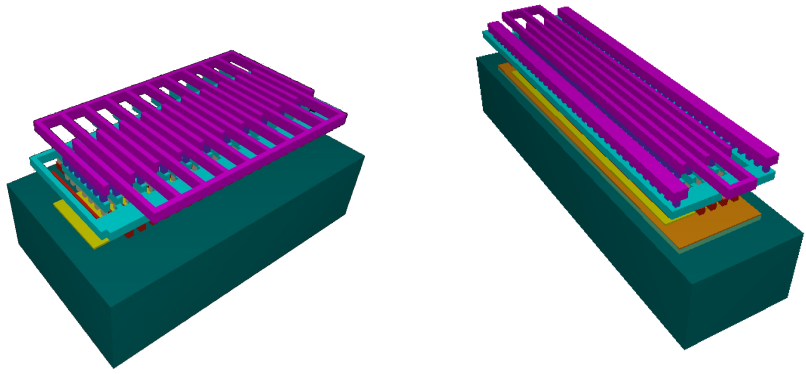


Figure 2.9: Different MOSFET finger widths, number of fingers and gate contact number will reduce the total gate resistance R_g

of the fingers cannot be reduced indefinitely, as for very narrow and short fingers, the increasing routing network and resulting $R_{interconnect}$ becomes dominant.

While minimizing the gate resistance has a positive influence on the f_{max}, the reduction in finger width will lead to an increase of total number of fingers. The corresponding increase in parasitic capacitance might initially be secondary to the reduction of R_g, but will become dominant once W_f is becoming too narrow. A transistor with a larger number of narrow fingers will have more gate-drain, gate-source and gate-bulk overlap capacitance (C_{gd}, C_{gs} and C_{gb}, resp.) than a transistor with the same total W with a few, wide fingers, as well as larger interconnection network to route and connect all the individual gate, source and drain traces. The increase in parasitic capacitance will lead to a decrease of the f_t, and will start to negatively impact the f_{max} once the gate resistance R_g is reduced so much that it is no longer dominant in Equation 2.6. In Appendix A.1, the impact of the routing network connecting the different gates on f_t and f_{max} is further explored. On top of this, the via resistance to connect the gate, drain and source to their routing layers, as well as any parasitic inductance of long traces of routing metals (in relation to the frequency) will further impact the high-frequency behavior of the transistor.

This can be illustrated by comparing the performance of two layouts of a transistor with the same total width (20µm), but different W_f and N_f ($20x1$µm and $4x5$µm). A 3D representation of both layouts is shown in Figure 2.10. Both transistors have a minimal gate length and gate contacts on both sides. The resulting f_{max} of the two layouts is shown in Figure 2.11: at their peak, the difference in f_{max} is close to 140GHz.



(a) (b)

Figure 2.10: 3D model representation of the two transistors with different finger width W_f

From the previous discussion, we can conclude that there is an optimal biasing point and transistor layout for high-frequency operation that balances both intrinsic as extrinsic/parasitic resistance, capacitance and inductance. As the extraction of all these components is not always straightforward, the usage of RF models is encouraged: RF transistor models are a type of simulation model of a transistor that are strongly linked to a predetermined layout, and which are fitted to actual measurement results. The remaining layout parameters when using RF models are generally W, N_F, L.

To demonstrate this optimum, an exploration of the design space of a 20µm wide and 40nm long NMOS transistor was conducted. The goal was to maximize the f_{max} by choosing the optimal W_f, N_F and biasing current. For a constant total finger width, different W_f and N_F transistors are designed and their gate biasing voltage swept. The drain of the transistor is always kept at the nominal supply voltage of 0.9V, and the bulk and source of the NMOS transistor are connected to ground. The resulting drain-source current I_{ds} is then normalized in relation to finger width to get the current density, and plotted on the Y-axis of Figure 2.12. The X-axis contains the individual finger width, and for each width and current density the corresponding f_{max} is plotted.

The design space exploration shows that the optimal individual finger width is around 1µm wide and a current density of 500µA/µm (or V_{gate} = 0.8V). Increasing the current density (by increasing the gate voltage) does not improve the f_{max}, as was previously shown in Figure 2.11. Reducing the gate resistance by narrowing the individual finger

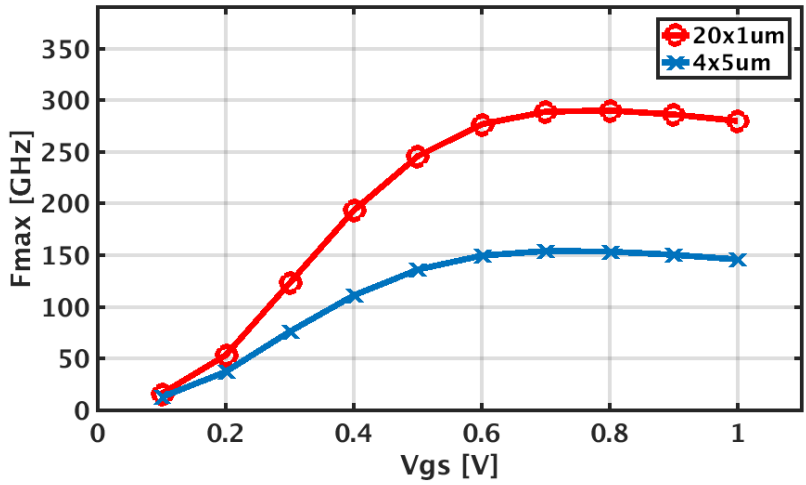


Figure 2.11: f_{max} curve of a NMOS transistor with different finger width but same total W, showing the impact of the gate resistance R_g on the high-frequency performance

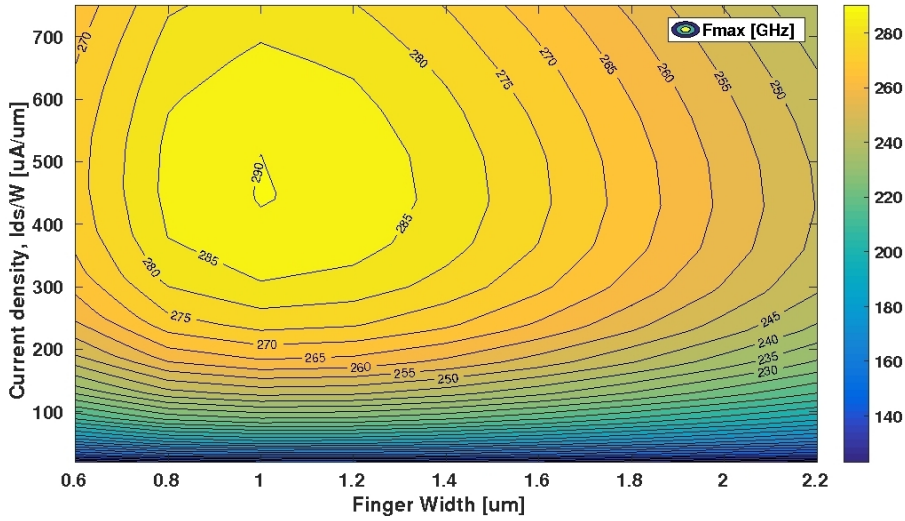


Figure 2.12: Simulated f_{max} of transistors with varying finger width (fixed minimal length of 40nm, fixed number of fingers of 20) and varying biasing point

widths leads to a higher f_{max}, but further decreasing W beyond the optimal finger width does not benefit the f_{max} as the vertical gate resistance and increased overlap capacitances become dominant again.

This section discussed the most important components of the transistor model and their influence on the high-frequency performance of the transistor. The strong dependence on layout, and the vast and complex parasitic component network means that the transistor design and layout process are intertwined and require extensive model extraction and optimization efforts. The simplified models and layout approaches utilized in digital and low-frequency design are not compatible with mm-wave and THz design, and will thus require a substantial amount of design time and attention.

2.3 Passive devices

Besides the active devices (transistor), many different passive devices are utilized when designing integrated circuits. In this section, an overview of the most commonly used passive components in THz circuit design is given. Performance and design trade-offs will be discussed, as well as equivalent models that provide additional insight in the behavior of the passive components in the mm-wave and THz band.

2.3.1 Metallization options

With increasing frequency, the required size and dimensions of the passive components becomes small enough to be integrated on chip instead of using off-chip components. This is especially true for inductors and transformers, components that are traditionally kept off-chip at low RF frequencies due to their large physical size. When designing passives, the metalization options of the process technology (or "metal stack") have a large impact on the performance that these on-chip passives can achieve.

The available metals in a typical CMOS process, as depicted in Figure 2.13, can be divided in three subgroups:

1. Lower metals: these metals range from metal layers one until five or six, and are mostly used for short interconnections. Their thickness is small (100nm$\sim$200nm), resulting in a larger series resistance when used over large distances. Their proximity to the substrate make these layers not optimal for implementing passives such as inductors or transformers at high frequencies.

2. Middle metals: multiple metal layers that are several times thicker than the lower metals (500nm$\sim$ 1μm), and can be used to route signals over longer

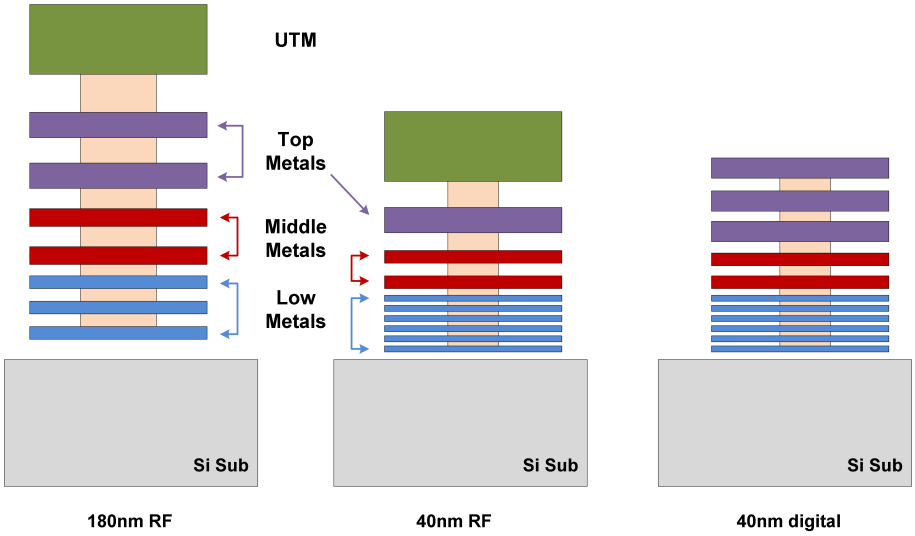


Figure 2.13: Example of a CMOS metal stack, with the lower, middle and top metal layers, for 3 different CMOS processes

distances without suffering too much losses due to the series resistance of the wire. Multiple middle metals can be combined in parallel to further reduce the series resistance.

3. Top metals: the top metals are the thickest metals of the metal stack, and are the furthest from the lossy silicon substrate. As a result, these are the layers where on-chip inductors and transformers are implemented, as well as global supply net distribution. A special case is the Ultra-Thick Metal layer (UTM-layer), where the highest metal layer is several μm thick. This low series resistance combined with the lowest coupling to the substrate makes the UTM layer the preferred layer for on-chip inductors, transformers, antennas and transmission lines at mm-wave and THz frequencies. Thanks to the increasing popularity of RF CMOS, metal stacks with UTM-layer options are available in most advanced process nodes, which was not always the case when RF/mm-wave/THz design was a mere afterthought due to the absolute dominance of digital design concerns.

The scaling of CMOS technology nodes does not only mean that the effective gate length decreases, but also has an impact on the metallization options available to the designer. The number of available metal layers has increased to cope with the rising interconnection difficulties that come with the ever-higher density of transistors.

Another major evolution is in the thickness of the different metal layers, and the corresponding proximity to the silicon substrate. The lower layer metal thickness has reduced to very thin traces of ≈100nm-200nm thin, with a significant rise in the trace sheet resistance [Shi10]. While the middle and top metal layer thickness has not changed that immensely in newer technology nodes, the reduction of the lower metals results in a closer proximity of the higher metals to the lossy substrate [Mam13]. The resistance of vias between metals, especially the lower metals, has also drastically increased for deep-scale nanometer CMOS technologies.

2.3.2 Inductors

Inductors are an important part of many circuits, especially oscillator circuits as they form a crucial part of the resonator tank. Starting from RF frequencies, it becomes practical to implement inductors on-chip as hollow spiral inductors [Cra97]; the higher the frequency, the smaller the required inductance and corresponding area footprint of the inductor. As a result, when designing oscillator circuits for THz transmitters, one can choose small single-turn spiral metal traces to act as inductors. Three parameters are important when designing an inductor: the inductance value L, the quality factor Q and the self-resonance frequency (SRF). The L and Q parameters are defined as follows:

$$L = \frac{\Im(Z_{11})}{\omega} = \frac{X_{Ind}}{2\pi f} \tag{2.8}$$

$$Q_{Ind} = \frac{\Im(Z_{11})}{\Re(Z_{11})} = \frac{X_{Ind}}{R_{Ind}} = \frac{\omega L}{R_{Ind}}, \omega \nearrow \Rightarrow Q_{Ind} \nearrow \tag{2.9}$$

The quality factor Q is an indication of the efficiency of the inductor. An ideal inductor has no energy losses, and would thus have a Q factor equal to infinity. However, all real inductors have some series resistance, resulting in energy losses and thus a finite Q factor. While designing an inductor, increasing the Q factor is usually a good idea as this will reduce the energy losses of the inductor.

Besides resistance, a real inductor also has some parasitic capacitance. This capacitance may come from any overlapping metals, fringe capacitance or capacitance to the substrate. While this (unwanted) parasitic capacitance tends to be small, it will form an LC-resonator with the (wanted) inductance of the inductor (Eq. 2.10). The frequency at which this resonance occurs is called the self-resonance frequency (SRF) and is a FoM indicating the parasitic capacitance of any given inductor.

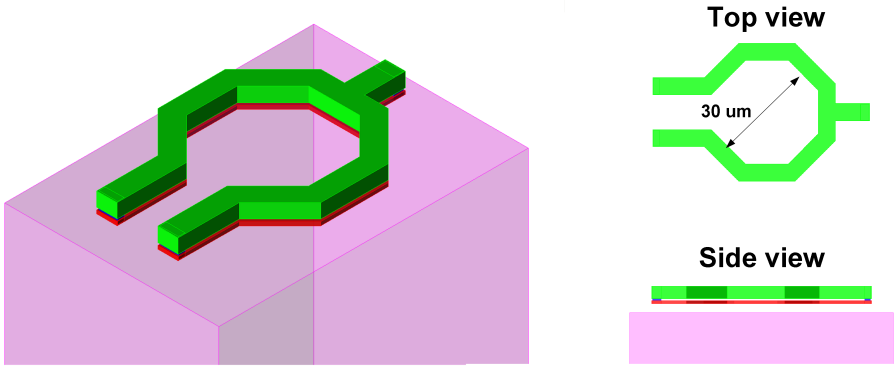


Figure 2.14: 3D model of a single-turn inductor, consisting of two top metals in parallel and an inner diameter of 30µm

$$SRF = \frac{1}{2\pi\sqrt{L_{Ind}C_{Ind}}} \tag{2.10}$$

A 3D representation of a single-turn inductor is depicted in Figure 2.14. This inductor has an inner radius of 30µm, a trace width of 5µm and is implemented in the two top metal layers of a 40nm CMOS technology, of which the highest metal is an UTM layer.

The corresponding inductance L and quality factor Q of this inductor are simulated using an EM simulator (ADS Momentum), and plotted in Figure 2.15. When evaluating the reactance of the inductor, it will be positive at frequencies below the SRF: this is the region where the component is inductive and looks and behaves like an inductor. The quality factor is positive. Around the SRF, the parasitic capacitances of the inductor start to form a resonant tank with the inductance, and the observed reactance peaks at the resonance frequency while the quality factor is equal to zero. Beyond the SRF, the reactance is negative and the capacitance of the inductor is dominant: the inductor is now functionally acting as a capacitor, and the quality factor becomes negative. For this particular inductor and utilizing Equations 2.8 and 2.9, the inductance at 200GHz is 72pH, the quality factor 20.5 and the self-resonance frequency around 495GHz.

To analyze the behavior of the inductor at different frequencies, the conventional single-π RF inductor model [Lon97] is modified to account for frequency-dependent resistive losses [Cao03]. Figure 2.16 shows the augmented single-π model, with indications of the frequency range where the different parts of the model come into play. There are three frequency regions, each with their own dominating loss mechanism:

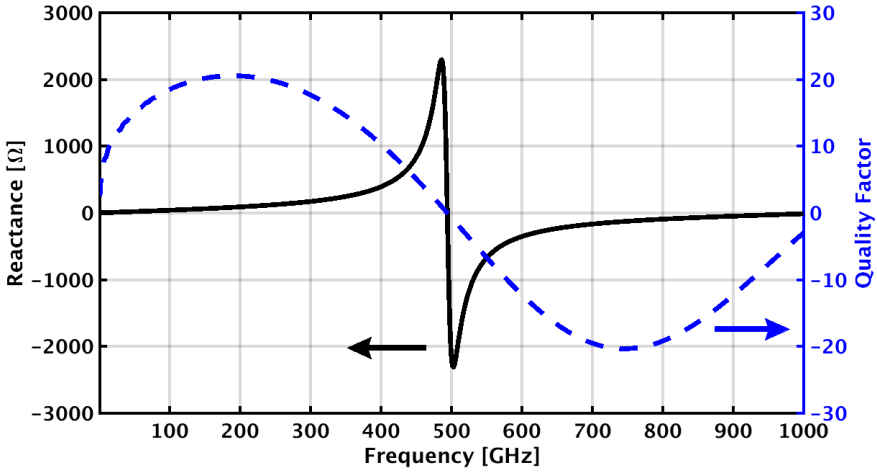


Figure 2.15: Reactance and quality factor Q of the single-turn inductor from Figure 2.14

- DC/low frequency: the device can be represented by inductor L_s in series with resistor R_s. The losses of the inductor are predominately due to the resistance of the metal trace(s) that form the inductor winding.
- RF/medium frequency: in addition to the conductive losses of the metal trace, frequency-dependent resistive losses should be accounted for at RF frequencies (skin effect and proximity effect). This can be implemented by adding the R_{skin}-L_{skin} network around R_s.
- At mm-wave/THz/high frequency, on top of the previously mentioned losses, the dominant loss mechanism is the substrate (C_{sub}//R_{sub}) and dielectric (C_{ox}) losses due to the conductive substrate under the inductor. By decreasing the substrate conductivity, the high-frequency eddy current losses in the substrate can be reduced. Low-loss substrates are available in GaAs and other III-V technologies, while Silicon-On-Insulator (SOI) CMOS technologies can achieve higher-quality passives as opposed to bulk CMOS technologies with their lossy silicon substrate.

In Figure 2.17, the quality factor of the inductor shown in Figure 2.14 is revisited with the impact of the different loss mechanisms for increasing frequency. From RF up to around 100GHz, the quality factor is dominated by the losses in the metal traces of the inductor. The quality factor of the inductor keeps increasing with frequency, which one

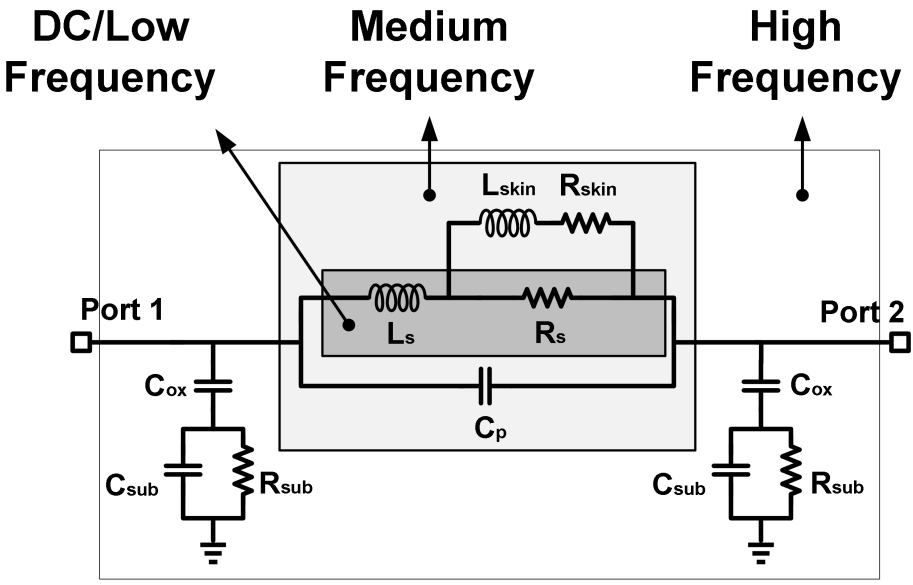


Figure 2.16: Single-π equivalent model of an inductor, with the relevant lumped components for different frequency regions [Cao03]

would expect based on the initial conclusion from Equation 2.9. Between 100GHz and 300GHz, the quality factor tops out and reaches it's maximum value around 200GHz. In this region, the substrate losses are becoming more and more important and stop the increase of quality factor with frequency. At even higher frequency, grip of the substrate losses on the quality factor tightens even further and changes the evolution of the quality factor to a negative trend with frequency.

To reduce the metal losses, the first thought would be to widen the metal trace, which will reduce the DC/low frequency series resistance. An alternative solution is to place several metal layers in parallel to achieve the same goal. However, both approaches will result in an increase in parasitic capacitance, which will in turn reduce the SRF. Using thicker metal traces would decrease the metal resistance with a much smaller impact on capacitance, and is the reason why passives are mostly implemented in the UTM/top metal layers, as these are the thickest and furthest away from the substrate.

The improvements in quality factor by increasing the trace widths also has it's limitations and diminishing returns: when the frequency rises, the current is seemingly forced to flow at the surface of the metal trace. This is called the skin effect, and results in a reduced effective cross-section of the conductor determined by the penetration

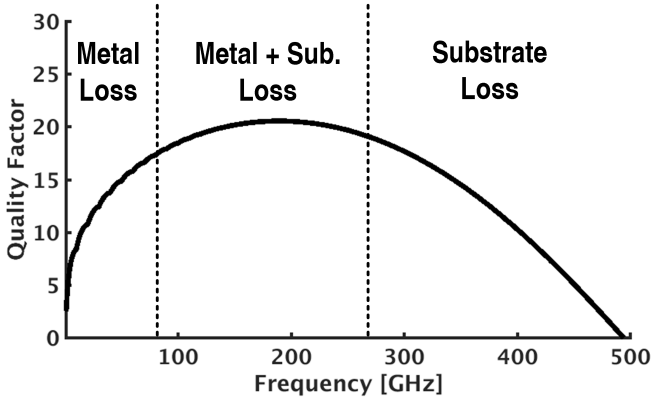


Figure 2.17: Quality factor versus frequency, with the dominant loss mechanisms for the different parts of the spectrum

depth or skin depth δ of the conductor at a certain frequency.

$$\delta = \frac{1}{\sqrt{\pi \cdot f \cdot \mu \cdot \sigma}} \tag{2.11}$$

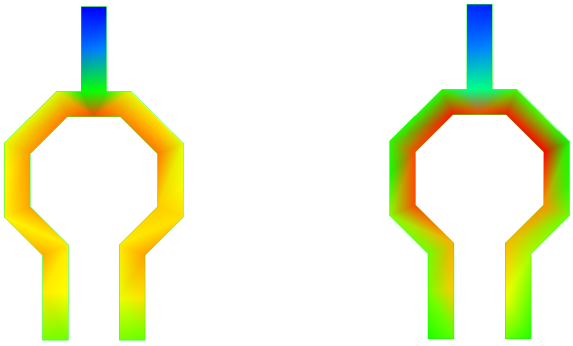
This skin depth becomes smaller with frequency, resulting in turn in an increase in resistance [Raz12]. For a copper conductor at 200GHz, using Equation 2.11 yields a skin depth of only 150nm. This will reduce any benefits gained from using wider metal traces to increase the effective conductor cross-section.

The magnetic field generated by the current in one trace of the inductor will in turn induce eddy currents in adjacent metals. These circular currents will influence the current distribution in the neighboring metal traces, as they add to the AC current on the inner side of the trace and subtract current on the outer side. This proximity effect or current crowding effect further lowers the apparent trace width and increases the effective series resistance of the trace. The frequency ω_{crit} where this current crowding effect starts to impose itself can be expressed as [Kuh01]:

$$\omega_{crit} = \frac{3.1}{\mu} \cdot \frac{W+S}{W^2} \cdot R_{\square} \tag{2.12}$$

Where W is the trace width, S the spacing between the two adjacent traces, μ the permeability and $R_{\square}$ the sheet resistance of the metal trace in which the inductor is fabricated. For a 5µm wide metal trace and a 30µm inner diameter, current crowding starts to occur at 12GHz. Just as with the skin effect, current crowding becomes

more prominent at higher frequencies, as is shown in Figure 2.18. In addition to a lower quality factor, current crowding will also reduce the inductance, as the effective diameter of the metal trace becomes smaller. As a result, the effective inductance will drop slightly compared to the low-frequency inductance with increasing frequency before starting to rise due to the SRF effect.



(a) (b)

Figure 2.18: Current crowding at the inner side of the inductor at higher frequencies (200GHz) (b) compared with DC (a)

The coupling to the substrate can be reduced by a patterned metal ground shield, implemented with narrow metal strips [Yue98]. While this can reduce the electric coupling to the substrate at high frequencies, this also increases the parasitic capacitance of the inductor and in turn reduces the self-resonance frequency. A patterned ground shield does not affect the magnetic coupling and resulting eddy currents in the substrate, which can only be reduced by increasing the substrate resistivity through additional process steps or a different choice in substrate material.

While the single-π model from Figure 2.16 is convenient to introduce the different loss mechanisms and overal inductor behavior, a more distributed model is preferred for high-frequency simulations. In addition, the single-π model loses accuracy at and beyond the SRF, as it does not anticipate the sign change of the real part of Y_{12} at high frequencies [Voi13b]. Figure 2.19 shows such high-frequency compatible equivalent model of an inductor, which is a double-π equivalent circuit [Hua06] with center tap connection. The derivation of the asymmetrical double-π model from the single-π inductor model can be found in Appendix A.2. In any case, 2.5D/3D EM simulator tools are essential for mm-wave and THz inductor analysis.

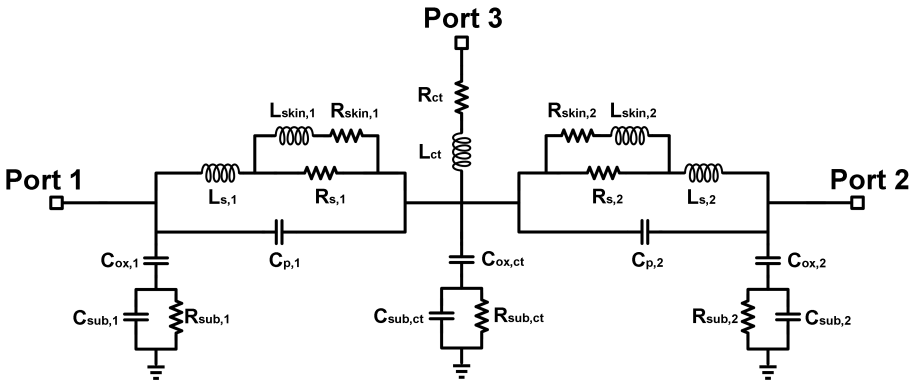
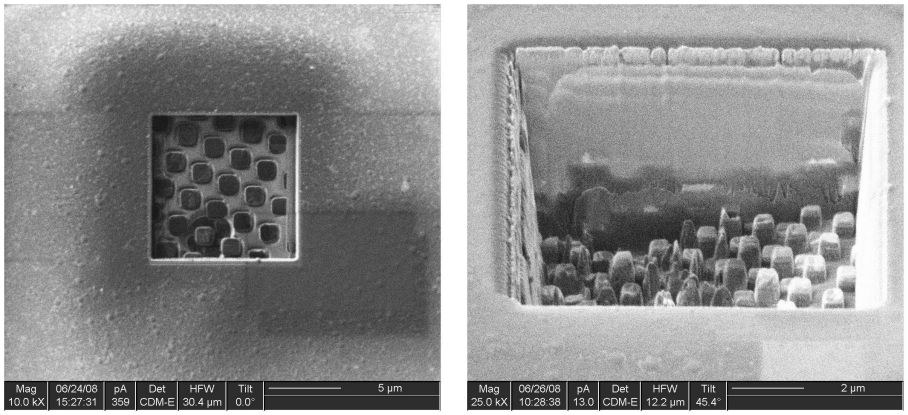


Figure 2.19: Equivalent double-π lumped-component model of an inductor with center tap, suitable for high-frequency analysis

2.3.3 Dummy-aware inductor and passive design

The importance of metal density rules in deep-scale nanometer CMOS technologies is becoming increasingly important, both production process-wise as for the design of high-frequency passives. When operating in the high-end of the mm-wave spectrum, passives become very small and the presence of nearby dummy metals has an increasing impact on the passives performance. Default dummy-filling tools aim to maximize the metal density in the whole chip (Figure 2.20), but this is not the goal of the passive designer: an automated dummy fill will change the behavior of the designed passive, whose impact is very difficult to verify due to enormous simulation time requirements. Dummy metals near transformers and inductors have a noticeable influence on their performance, as has been reported up to 60GHz [Zha13, Tsu08, Nan07]. In the following section, the impact of these dummy metals on inductors beyond 60GHz will be discussed (a similar analysis can be done for other passives). The results will be compared at RF, mm-wave and THz frequencies [Ste17].

The foundry-provided dummy filling tool aims to generate a 80-90 percent metal density, and yields a dummy-filled layout as depicted in Figure 2.21. While this high, uniform metal density is good to minimize any process-related variations, it is virtually impossible to simulate due to the mesh of very narrow metal strips. To analyze the impact of different dummy metal densities at (sub-)mm-wave frequencies, a fixed dimension dummy unit structure is manually placed to achieve 10 to 40 percent metal density (as shown in Figure 2.22) around an inductor with 15µm inner diameter and 5µm trace width. Each unit dummy structure consists of a 2.4µm x 2.4µm metal square of all consecutive dummy metals. The structures are spaced evenly to achieve the

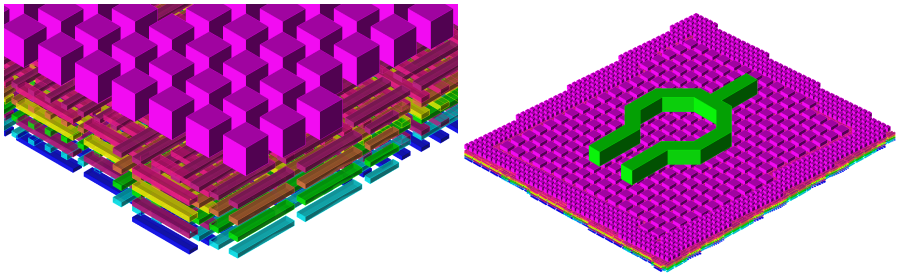


(a) (b)

Figure 2.20: Scanning electron microscope (SEM) photo of top metal dummy structures, made visible by removing the top passivation layers with a focused-ion beam (FIB)

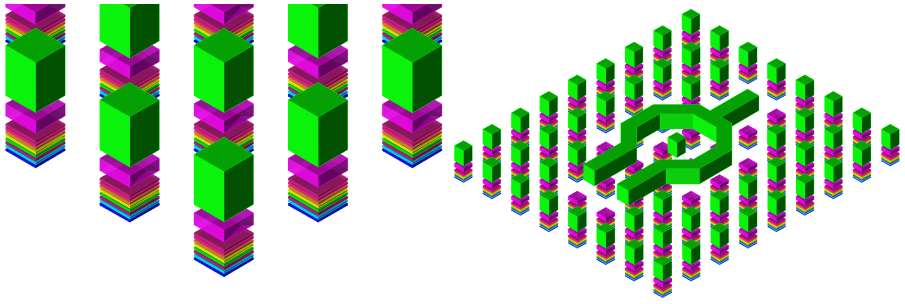
desired density, and the inductor is implemented in the top UTM layer and simulated in a 2.5D EM simulator (ADS Momentum). Several other unit dummy structures have also been used, differing in both size (1.2µm x 1.2µm and 4.8µm x 4.8µm) and metal stacking structure (stacked on top of each other or in a staircase-like spiral). While the inductor performance of these different unit dummy structures do not vary much for the same total density, there is a huge difference in simulation time: a 10% density fill with 2.4µm x 2.4µm squares is almost 40 times faster to simulate than 1.2µm x 1.2µm squares, with less than 1% variation in the results. Consequently, 2.4µm x 2.4µm squares are used as they allow relatively fast simulations while maintaining high simulation accuracy. An overview of the different unit dummy structures used and their results and simulation time can be found in Table A.3 in Appendix A.3.

The resulting simulated inductance L and inductor quality factor Q for different dummy metal densities are shown in Figure 2.23. While the inductance does not vary greatly, an extensive divergence is seen when looking at the quality factors of the various metal densities: the difference in quality factor with and without dummies increases at higher frequencies. At RF frequencies, the impact of the dummy metals is minimal, while a noticeable difference is detectable at mm-wave frequencies. The spread in quality factor between 0% and 40% dummy fill is 25% at 80GHz, while at 200GHz, adding 40% of dummies decreases the total quality factor by half compared to the same, dummy-free inductor. Clearly, this shows that dummy metals have a significant impact on the behavior of mm-wave and certainly THz passives. A minimum of dummy metals should be pursued and these dummy metals should be placed manually for the critical



(a) (b)

Figure 2.21: Close-up of an automatically filled dummy pattern (a) and the automatic placement around an inductor (top metal dummies are not shown) (b)

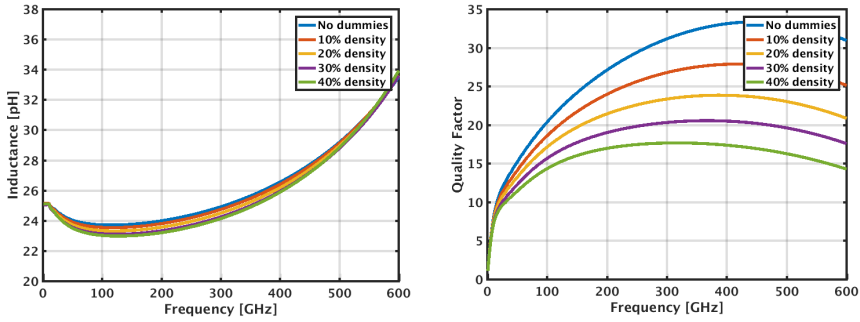


(a) (b)

Figure 2.22: Close-up of a 10% manual dummy fill unit structure and the placement around an inductor

high-frequency components.

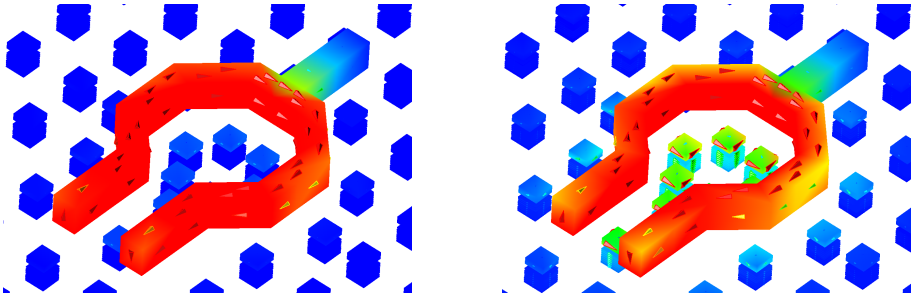
The dominant loss mechanisms due to dummy filling are the magnetically induced eddy currents in the dummy metal structures and the additional capacitive coupling to the lossy silicon substrate. Figure 2.24 shows the current distribution of the same inductor with 10% metal dummy density for different frequencies. At low frequency (10GHz), the losses of the inductor are dominated by the resistive losses of the metal inductor trace and the eddy currents in the dummy metals are minimal. At mm-wave frequencies, the magnetic field of the inductor starts to induce observable eddy currents in the top layers of the dummy structure. From this point on in the frequency spectrum, the dummies start to have a substantial impact on the quality factor of the inductor. At higher frequencies (200GHz and 300GHz), the dummy structure becomes a capacitive path to the substrate, further increasing the total parasitic capacitance to the substrate



(a) (b)

Figure 2.23: Simulated Inductance L (a) and quality factor Q (b) for inductors with different dummy densities

and lowering the SRF of the inductor. The losses are now both the eddy currents being induced in all metal layers of the dummy structure, as well as the increased coupling to the lossy silicon substrate. To verify that a major part of the losses is due to the metal dummies themselves and not due to the extra coupling to the substrate, an inductor without substrate and 0%/30% dummies is simulated (Table A.3). The difference in inductance between the two cases remains small (removal of the substrate reduces the effective inductance), but the quality factor drops with almost a third at 200GHz due to eddy currents.



(a) (b)

Figure 2.24: Current distribution in the dummy structures for different frequencies: 10GHz and 200GHz, additional frequencies shown in Figure A.8

The importance of the losses due to eddy currents in the dummy metals prompts the question for the otimal way of placing the dummies. Two main approaches are

compared:

- An even distribution, where the unit dummy structures are placed on an evenly spaced grid. As a result, some dummy units will be (partially) overlapping with the inductor trace, and a few will be positioned inside the inductor winding.
- A "trace clear" distribution (TC), where the designer takes care to not place any dummy structures directly under the metal trace of the inductor. As this means that the space under the trace is devoid of dummy metals, additional dummy structures will have to be placed inside the winding of the inductor to meet the minimal local density requirements.

As the magnetic field in a differentially driven inductor is the largest inside of the inductor winding, placing more dummy structures between the traces in the TC approach will result in larger eddy currents being induced, and as a result larger losses. This effect grows when higher dummy densities are applied. Current distribution simulations can be found in Figure A.7. The difference between an even distribution and a TC design, however, can be kept small by minimizing the number of dummy structures inside the inductor winding.

2.3.4 Transformers

Similarly to the rise of on-chip inductor usage, the increase in operating frequency has enabled the reduction of transformer size, meaning that they can be implemented on-chip without an enormous area penalty [Lon00]. Transformers can be used for galvanic separation between two parts of a circuit and bias the circuits connected to the primary and secondary winding differently when equipped with a center tap. Transformers have also been used for on-chip power combining [Aok02] or impedance matching [Wan10], and have become an essential component in the designer's toolbox when designing at mm-wave frequencies [Cho09] [Def10].

The transformer consists of two magnetically coupled inductors (L_p and L_s). Consequently, the same performance parameters to describe an inductor can be used to evaluate the primary and secondary winding of the transformer (quality factors Q_p, Q_s and SRF_p, SRF_s). The coupling coefficient k indicates how tightly the primary and seconday winding are coupled with each other. The maximum is reached when $\mid k \mid = 1$. The coupling factor can be calculated from the simulated Z-parameters using Equation 2.13:

$$k = \sqrt{\frac{\Im(Z_{12})^2}{\Im(Z_{11}) \cdot \Im(Z_{22})}} \tag{2.13}$$

When transformers are used to transfer power from one stage of the circuit to another, a non-ideal transformer will lose some of this power. This insertion loss should be kept to a minimum to increase the efficiency η of the transformer. Equation 2.14 shows that η depends on the coupling factor k and the quality factor of the transformer windings.

$$\eta = \frac{1}{1+2\sqrt{(1+\frac{1}{Q_p Q_s k^2})\cdot\frac{1}{Q_p Q_s k^2}+\frac{2}{Q_p Q_s k^2}}} \tag{2.14}$$

$$\eta = 10^{MAG/10} \tag{2.15}$$

The G_{max}/MAG of a transformer indicates the maximum gain (=miminal insertion loss), and is always lower than 0dB as the transformer is a passive component. This optimal case for minimal insertion loss can only be attained if both input and output of the transformer are perfectly matched, and is thus an upper limit of the performance that a real transformer can achieve in any real circuit.

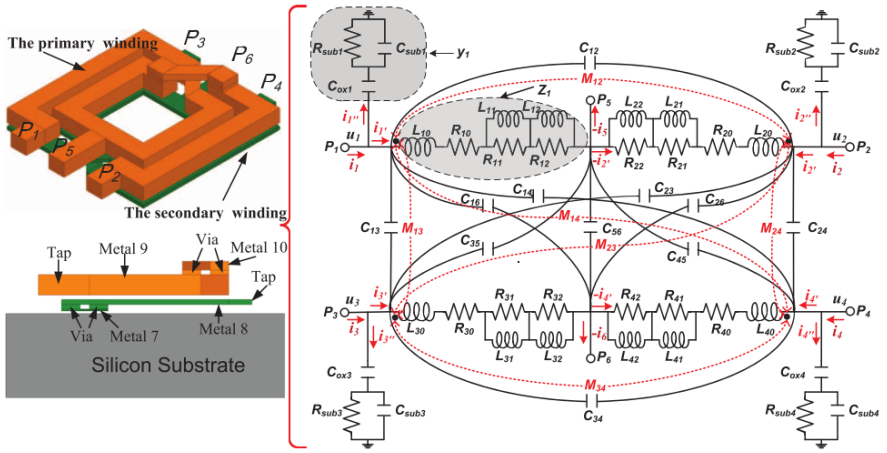


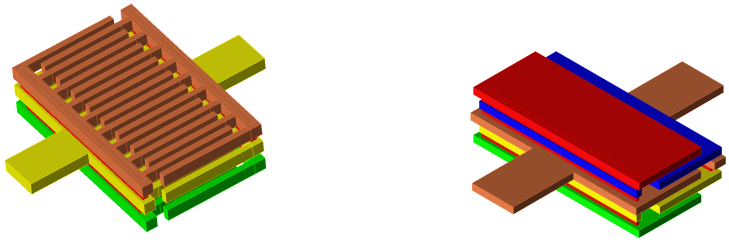
Figure 2.25: Image of a transformer in CMOS and the equivalent high-frequency model [Gao15]

Figure 2.25 shows an on-chip transformer in a CMOS process, together with its equivalent high-frequency model. The basis of this lumped-component model are two inductor models with additional magnetic coupling between the different inductive parts of the transformer windings, as well as extra coupling capacitors between the two transformer winding traces. Similar loss mechanisms as for inductors (Section 2.3.2) should also be accounted for in the transformer model, such as series resistance,

skin effect, proximity effect and substrate losses. The model complexity and accuracy remains a difficult aspect at THz frequencies, and requires extensive 3D EM simulations and an iterative design flow to be effectively used in sub-mm-wave circuits and designs.

2.3.5 Capacitors

Capacitors in a CMOS process can be divided between fixed-value and tune-able capacitors. Metal-Oxide-Metal capacitors, or MOM-caps, are a series of interweaved metal fingers (comb) or plates close to each other spaced by oxide material, with the intent to create an overlap capacitance (Figure 2.26). By placing very small, narrow fingers very close to each other, and by using many different metal layers, a high capacitance density can be obtained. MOM-caps have a fixed, non-tuneable capacitance, and are included as standard components in most CMOS design kits.



(a) (b)

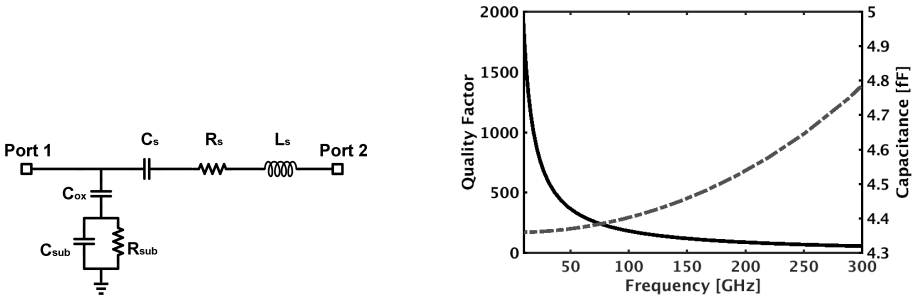
Figure 2.26: 3D model representation of MOM-capacitors with fingers (a) or plates(b)

Another fixed capacitor type in CMOS is the Metal-Insulator-Metal (MIM) capacitor, which utilizes a thin, high-k insulating layer between two metal plates to achieve a high-quality capacitor. However, this requires additional process steps and as such availability depends on the chosen metallization options in the CMOS process.

Varactors, on the other hand, are variable capacitors where the effective capacitance can be modified by changing the applied voltage. This variable capacitor is a very useful component in oscillators, since it allows the tuning of the oscillation frequency by changing the LC product of the tank. Available varactor types are Accumulation-mode MOS (A-MOS) varactors and pn junction (diode) varactors.

Just like inductors, the efficiency of a capacitor can be expressed through a quality factor which is strongly dependent on frequency:

$$C_{Cap} = \frac{\Im(Y_{11})}{\omega} = \frac{1}{2 \cdot \pi \cdot f \cdot X_{Cap}} \tag{2.16}$$



(a) (b)

Figure 2.27: Equivalent capacitor model (a) and simulated capacitance (dotted line) and quality factor (solid line) of a MOM-capacitors with interlocking fingers (b)

$$Q_{Cap} = \frac{\Im(Y_{11})}{\Re(Y_{11})} = \frac{X_{Cap}}{R_{Cap}} = \frac{1}{\omega \cdot C_{Cap} \cdot R_{Cap}}, \omega \nearrow \Rightarrow Q_{Cap} \searrow \tag{2.17}$$

By examining Equation 2.17, one can see that the quality factor of a capacitor decreases at higher frequencies, which is the opposite trend observed with the inductor (Equation 2.9). This is the main reason why for THz design, capacitors (and especially varactors) suffer from a very low quality factor and are therefore less used compared with RF/mm-wave designs. The majority of capacitors used in THz circuit design are parasitic capacitances which are re-purposed to serve a useful function in the circuit.

The lumped component equivalent model of a capacitor is shown in Figure 2.27, and can be used for both MOM-caps, MIM-caps and varactors (by replacing the fixed C_s with a variable capacitor). In Figure 2.27 b, the simulated capacitance and quality factor of a 4.5fF MOM-cap with comb-like fingers are shown. While the quality factor at low frequency is very high, it sharply decreases with increasing frequency. The capacitance is also slightly rising: this is due to the SRF of the capacitor, as the parasitic inductance of the capacitor forms a resonant tank at high frequencies, in a very similar fashion as with an inductor.

2.3.6 Transmission Lines

As the wavelength of a signal is inversely related to the frequency, metal traces and interconnect dimensions are becoming the same order of magnitude as the wavelength at mm-wave and THz frequencies. Whereas these traces can be ignored or represented as a simple lumped component model at low frequencies, this is not longer possible at

high frequencies. These traces should now be represented by a distributed equivalent transmission line (TL) model. Transmission lines play an import role for matching, as they can provide impedance transformations with a large range by changing the length, width and spacing of the transmission line traces. The most important parameters to characterize a TL are the characteristic impedance Z_0, wave velocity υ and the propagation constant γ, which consists of the attenuation constant α and the phase constant β (Equations 2.18 - 2.21). The phase constant determines how much phase rotation will occur for a certain length of the TL, and thus determines the rotation on the Smith chart when doing impedance matching. Figure 2.28 shows a 3D model of a differential transmission without/with slow-wave strips, as well as an equivalent model for an infinitesimal transmission line segment Δx, containing a series resistor R and inductor L and a shunt capacitor C and admittance G. For a lossless TL ($R, G = 0$) and/or at very high frequency, the equations for Z_0 and υ can be simplified to only depend on the inductance and capacitance of the TL.

$$Z_0 = \sqrt{\frac{R + j \cdot \omega \cdot L}{G + j \cdot \omega \cdot C}} \approx \sqrt{\frac{L}{C}} \tag{2.18}$$

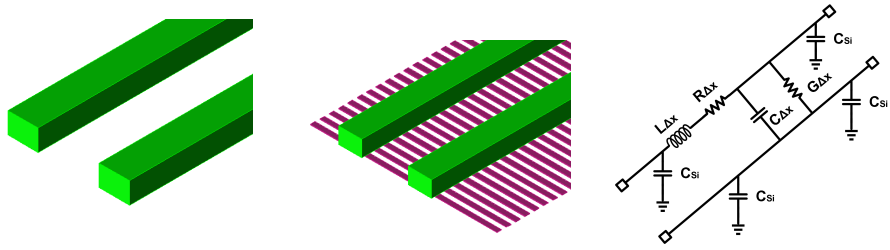
$$\upsilon = \lambda \cdot f \approx \frac{1}{\sqrt{L \cdot C}} \tag{2.19}$$

$$\gamma = \alpha + j\beta \tag{2.20}$$

$$\beta = \frac{2 \cdot \pi \cdot f}{\upsilon} = \omega\sqrt{L \cdot C} \tag{2.21}$$

The slow-wave variant of the differential transmission line is one where under the transmission line, narrow metal strips are placed orthogonal to the TL direction (Figure 2.28b). The addition of these metal strips increases the capacitance C of the TL, and thus reduces the wave velocity υ hence the name "slow-wave transmission line" (SWTL). As a result, the phase constant β increases and the needed TL length decreases, providing a shorter transmission line compared with a conventional TL with the same phase rotation. The addition of the patterned metal shield introduces some additional losses, but can reduce the area occupation (and resulting cost) of transmission lines with large phase rotation.

The characteristic impedance Z_0 and propagation constant γ can be calculated using ABCD-paramters (Section A.4), which in turn can be derived from measured/simulated S-parameters.



(a) (b) (c)

Figure 2.28: Differential transmission lines: conventional TL (a) and slow-wave TL (b) and the equivalent model for a infinitesimal segment (c)

2.4 Conclusion

In this chapter, the many active and passive components that are commonly used in THz circuits design have been introduced and their THz behavior has been highlighted. In Section 2.2, the design and layout optimization of the CMOS transistor for high-frequency operation has been discussed, showing the different trade-offs when designing circuits at the edge of the technology's capabilities. In Section 2.3, many different types of passives that can be implemented in a CMOS process have been discussed. Their performance changes drastically at mm-wave and THz frequencies and thus requires extensive attention and modeling of effects that are negligible at lower frequencies. The impact of dummies, a standard 'design for manufacturability' (DFM) requirement from foundries, has been evaluated specifically on inductors at THz frequencies.

Overall, the modeling of both active and passive components has become very critical and complex at THz frequencies. Special designer attention, understanding of the different loss mechanisms of the used components and tools, such as parasitic extraction (PEX) software (Calibre/Assura) and 3D EM simulators (Momentum/EMX/HFSS), are a necessity when designing circuits for the THz frequency spectrum.

Chapter 3

Antennas and IO

After generating the high-frequency signals on-chip, the next step is to get them off-chip to be measured. In a real-world application, the THz signals will eventually reach an antenna to interact with objects (imaging) or other chips (communication). In the following sections, different ways of getting signals on and off chips will be shown and their usefulness for THz electronics discussed.

3.1 Bondwire and FlipChip

Bondwires are a tried-and-true interconnect method, used for bringing DC and low-frequency signals on-chip. Using this method, a conductive wire (aluminium or gold) is drawn between the on-chip bondpad and a trace on the target board or other chip, as shown in Figure 3.1. While this is a cheap, mature and effective way of getting signals on/off chip at lower frequencies, their use becomes less straight-forward at mm-wave frequencies. Bondwires can be represented by an equivalent model very similar to that of an inductor, connecting the on-chip bondpad to the off-chip signal trace of the package. Just like the inductor from Section 2.3.2, bondwires can be characterized by their inductance, quality factor and self-resonance frequency. At DC levels, the bondwire acts as a low-impedance path to the chip, determined by the series resistance of the bondwire itself. As the material used (Au and Al) have a very high conductivity, the length of the inductors has a limited impact on the voltage drop between off-chip and on-chip biasing voltages. As the frequency increases, the impedance (both real and imaginary parts) of the bondwire increases: the skin and proximity effect starts to negatively impact the resistive properties of the bondwire, while the reactance becomes larger due to the influence of any parasitic capacitance and the SRF. If left unchecked, the bondwire will act as an RF choke inductor, blocking any high-frequency signals to and from the chip.

This is not to say that bondwire interconnects are not possible at mm-wave frequencies: by reducing the bondwire length, the inductance of the wire and corresponding SRF will decrease. As a rule of thumb, a 1mm-long bondwire has an inductance of 1nH.

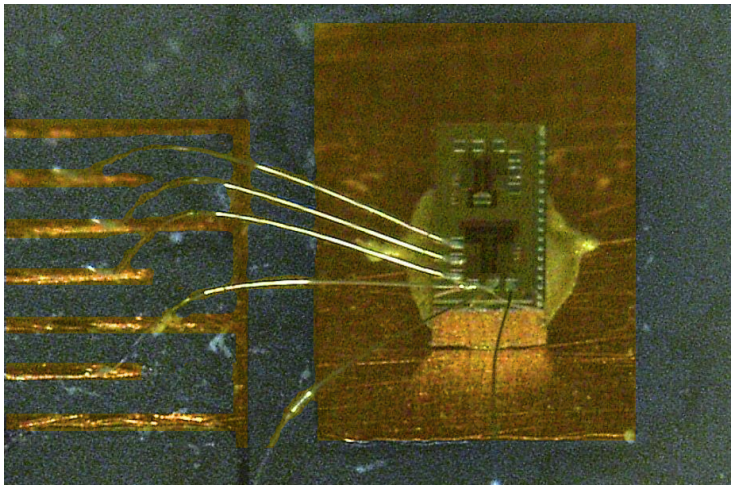


Figure 3.1: Bondwires used to connect a THz chip to on-board metal traces for DC biasing

The change in complex impedance of the bondwire can also be compensated by applying matching techniques and other impedance transformations. Compensated bondwire interconnects have been demonstrated at mm-wave for chip-to-microstrip interconnects [Liu11], and have been shown to operate far above 100GHz [Val15]. However, the bondwire length should be drastically reduced, which increases the packaging complexity.

Another popular packaging technique is flip-chip, where the die is provided with (gold) solder balls or studs on the pads, flipped over, aligned with the traces on the carrier board and then pressed against the board while the solder balls are re-melted to realize the electric connection between trace and pad [Jen01]. Figure 3.2 depicts the cross-section of a flip-chip interconnect, as well as an equivalent model of the gold ball interconnect [War02]. The inductance of the gold studs is determined by their height, which is around 50pH for a 20µm high solder ball. Multiple gold studs can be stacked on top of each other if required, but this reduces the mechanical integrity of the die-board connection. For the purpose of THz interconnection solutions, the flip-chip solder balls can be viewed as a bondwire solution [Kha14] where the bondwires are only 20μm long, thus increasing the SRF, reducing the series losses and impedance transformation ratio compared to bondwires. As a result, flip-chip interconnects can facilitate the transmission of high-frequency signals on- and off-chip and are easier to compensate for the varying complex impedance with increasing frequency. Flip-chip interconnects have been demonstrated above 200GHz [Mon15], but start to run into practical implementation problems, mainly on the package board side: the

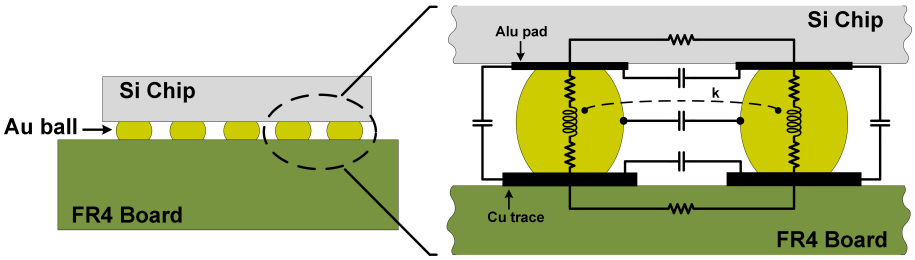


Figure 3.2: Die-to-board flip-chip cross-section (left) and the equivalent model of the flip-chip interconnect (right)

minimal trace width and pitch will determine the on-chip pad pitch and the required on-chip connections between these pads, which all become transmission lines in the THz frequency range. If this spacing and resulting on-chip interconnection network becomes too large compared to the wavelength of the transmitter signal, the matching losses will become too large and result in an inefficient interconnect.

For a good comparison between the two approaches for mm-wave applications, the same E-band amplifier is packaged using bondwires [Zha15] and flipchip [Zha16b], where flipchip achieves better performance. While both bondwires and flip-chip are packaging techniques that extend to the mm-ave and THz range, their practical usability is rather limited and as such other packaging or measurement solutions are required at THz.

3.2 Probes

The most direct and accurate way of characterizing a signal generated on-chip is by using probes and directly measuring the signal at the on-chip pads. At mm-wave Ground-Signal-Ground (GSG) co-planar probes are commonly used to characterize the performance of individual circuit blocks, such as amplifiers and oscillators. When the measured signal goes to higher frequencies, the pitch between these GSG probe pads decreases to accommodate the narrowing probe tip pitch while maintaining adequate spacing and minimal size to conform with the process' design rules. As these probe pads are relatively large metal planes in close proximity of each other, they have both parasitic capacitance to the substrate as fringe capacitance with the surrounding metals and other probe pads. In [Def13], an equivalent model of a GSG pads is proposed, showing that the size of these pads also has an influence on the performance of the output circuit and should be included in the output matching network. EM

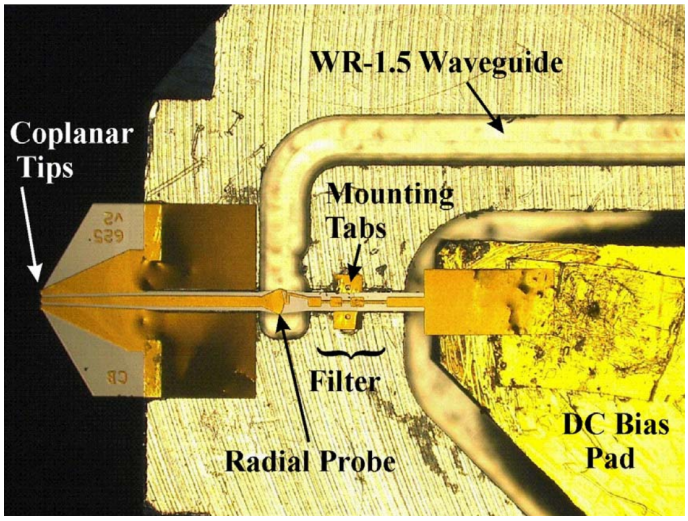
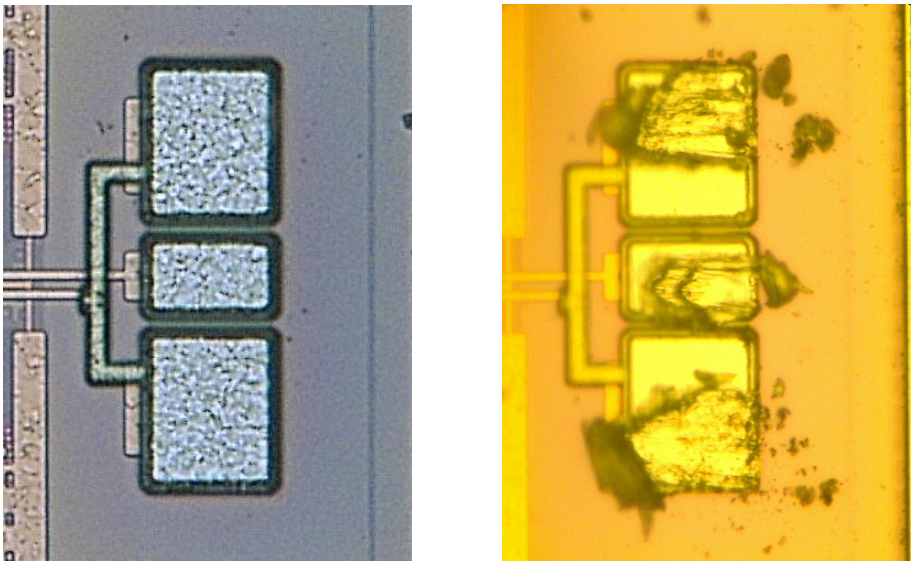


Figure 3.3: Cross-section of a WR1.5 probe used to measure circuits operating from 500-750GHz [Wei11]



(a) (b)

Figure 3.4: GSG probe pads before and after being probed using a WR5.1 probe, clearly showing the landing marks on the top metal layer

simulations of the probe pads are necessary at THz, as the probe pads can be considered as electrically large compared to the signal wavelength. Nonetheless, direct on-wafer probes are available up to 1.1THz [Bau14], and the cross-section of a WR 1.5 probe is shown in Figure 3.3.

Another point of concern is the limited repeatability of measurements with probes on the same die: repeated landing of probes on the same small probe pads will scratch the top aluminium layer of the probe pads (Figure 3.4), meaning that there is a limited amount of probe landings a GSG pad can handle before becoming too damaged to measure consistent results. On top of this, the precise position of the probe tips in the probe pads is also not always exactly the same, which could result in small differences in measurements.

The fact remains that on-chip probing remains one of the most direct and precise measurements that can be done to measure the performance of an electronic circuit. However, due to the very high cost of probes, the fragile mechanical components and the need of an expensive, bulky probe station, the usage of probes is only done in a controlled laboratory or testing environment and cannot be used in a real world application.

3.3 The need for THz antennas

3.3.1 Introduction to antennas

In any wireless communication or imaging system, antennas are the passive components that will convert the electrical signals on-chip into electromagnetic (EM) waves. These EM waves will then propagate through the channel medium (usually air, but this could be other materials) towards the target, which could be the antenna of a receiver (communication) or an object (imaging). Antennas are reciprocal devices [Nei43], meaning that the the transmitting and receiving characteristics of an antenna are the same: the radiation pattern and efficiency does not change whether an antenna is used to transmit or receive signals.

To adequately discuss and compare antennas at THz, some basic concepts and definitions [Joh84] are given in the following section. One of the most important properties of an antenna is how much power is being radiated in a specific direction. Using a spherical coordinate system, the radiation intensity $U(\theta,\phi)$ denotes the radiant flux (radiant power) in a certain direction, in watts/steradian. The total radiated power P_r is the sum of all the radiant power in all directions from the source antenna, expressed through a spherical integral over θ and ϕ.

$$P_r = \int_0^{2\pi} \int_0^{\pi} U(\theta,\phi) sin(\theta) d\theta d\phi \tag{3.1}$$

A special case in antenna theory is the isotropic antenna: this is an antenna which has the same radiation intensity in all directions, and whose radiation pattern would form a perfect sphere. The intensity $U(\theta,\phi$ in all directions would be equal to the average radiation intensity U_{avg}:

$$U_{avg} = \frac{P_r}{4\pi} \tag{3.2}$$

Using the ideal isotropic antenna as a reference, we can define the directivity $D(\theta,\phi)$ of an antenna as the ratio of its radiation intensity in a certain direction to the radiation intensity of an isotropic antenna. This property expresses how much of its total radiated power the antenna can concentrate in a specific direction. Since this is the concentration of radiation intensity in relation to that of an isotropic antenna, this is expressed by using the unit decibels-isotropic (dBi). Considering that this is the most common way to express antenna directivity and gain, dB and dBi will be used interchangeably in this work when discussing antenna directive properties.

$$D(\theta,\phi) = \frac{U(\theta,\phi)}{P_r/4\pi} \tag{3.3}$$

As with any real passive device, antennas are non-ideal and thus suffer from various losses. As a result, not all power delivered to/accepted by the antenna (P_a) is converted to radiated power (P_r). This ratio is the radiation efficiency η_{rad}, and is determined by any dielectric or conductor losses of the antenna, as well as substrate and surface wave losses. A higher η_{rad} means more electrical power being converted to wanted, radiated power.

$$\eta_{avg} = \frac{P_r}{P_a} \tag{3.4}$$

By combining the directivity and efficiency, we can define the gain $G(\theta,\phi)$ of an antenna, which describes how well the antenna can convert and focus the accepted power into radiated power in a specific direction.

$$G(\theta,\phi) = \eta_{rad} \cdot D(\theta,\phi) = \frac{\eta_{rad} \cdot U(\theta,\phi)}{P_r/4\pi} = \frac{U(\theta,\phi)}{P_a/4\pi} \tag{3.5}$$

If the antenna was a lossless component, all of the accepted power would be converted to radiated power, the radiation efficiency would be 100% and the directivity and gain would be equal. Note that the accepted power used to calculate the radiation efficiency does not include any matching losses due to reflections, and should be accounted for when integrating the antenna in the rest of the circuit. When working with antennas, the designer is most interested in the peak directivity and peak gain of the main radiation lobe. Therefore, unless mentioned otherwise, the use of "directivity" and "antenna gain" will refer to these peak values.

As mentioned earlier, an isotropic antenna radiates the same amount of power in any direction. Using Equation 3.3, we find that the directivity in all directions is 1 or 0dB, which is the theoretical lower limit for directivity. This perfect isotropic radiator is a purely theoretical concept, since the implementation of it is impossible due to not simultaneously meeting the Helmholtz Wave Equations in all directions [Wik17]. The impossibility of an isotropic radiator is an example of the "Hairy Ball Theorem" [Bro12] [Mil78], which states that for a continuous vector field tangent to the surface of a sphere, there have to be one or more points where the vector field reduces to zero. As the electric and magnetic field of the radiated EM waves are orthogonal to the direction of propagation, an isotropic radiator would require a continuous vector field consisting of the E and B fields tangent to the surface of the radiation sphere around the antenna.

Therefore, any real antenna will have a point in the radiation pattern where more power is radiated than the average radiation intensity, and thus will have a peak directivity larger than 0dB. The gain of an antenna, however, can drop below 0dB as any losses will degrade the radiation efficiency.

3.3.2 Implementation and challenges at THz

Link budget and Free-Space Path Loss

When designing a wireless communication or imaging system, it is important to know how much power will be received by the target for a certain transmitter output power. This link budget analysis can be done using the Friis transmission formula [Fri46], given by Equation 3.6.

$$\frac{P_R}{P_T} = G_T \cdot G_R \cdot \left(\frac{\lambda}{2 \cdot \pi \cdot d}\right)^2 \tag{3.6}$$

In this link budget equation, the ratio of the received power P_R to the transmitted power P_T depends on the antenna gain of both transmitter (G_T) and receiver (G_R) antenna, as well as the Free-Space Path Loss (FSPL). This last part of the equation is a virtual

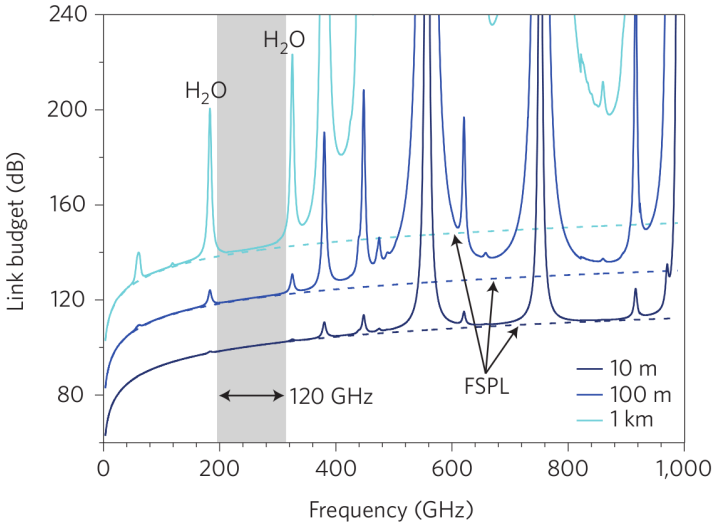


Figure 3.5: Free-space path loss for different distances over the frequency range [Nag16]

loss, and is due to the spreading of the electromagnetic waves in free space as it travels further and further away from the source.

$$FSPL = \left(\frac{4 \cdot \pi \cdot d}{\lambda}\right)^2 = \left(\frac{4 \cdot \pi \cdot d \cdot f}{c}\right)^2 \tag{3.7}$$

$$FSPL_{dB} = 10 \cdot log_{10}\left(\frac{4 \cdot \pi \cdot d \cdot f}{c}\right)^2 = 20 \cdot log_{10}(d) + 20 \cdot log_{10}(f) - 147.55 \tag{3.8}$$

The FSPL is dependent on both the frequency (in Hertz) of the signal being transmitted and the distance (in meters) between the transmitter and receiver. For a 300GHz signal, the FSPL is 76dB at 0.5m and 102dB for a distance of 10m. For short-range distances (up to 10m), the atmospheric attenuation is negligible compared to the FSPL except for the largest H_2O resonance peaks (557GHz and 752GHz), as shown in Figure 3.5. At THz frequencies, the FSPL is the dominant limiter of effective transmission distance for most applications, and the range will thus be limited to several meters.

As antenna parameters and FSPL are commonly expressed in dB, the Friis transmission formula can be rewritten to:

$$P_{R,dBm} = P_{T,dBm} + G_{T,dB} - FSPL_{dB} + G_{R,dB} \tag{3.9}$$

The link budget formula is only compatible with both transmitter and receiver antennas operating in the radiation far-field region. In this region, the radiation patterns do not change with distance (but the power density does due to FSPL). The distance of the boundary between the radiating far-field (Fraunhofer) region and radiating near-field (Fresnel) region is defined by the following conditions, which must all be met:

$$d > \frac{2 \cdot D_{im}^2}{\lambda} \tag{3.10}$$

$$d >> \lambda \tag{3.11}$$

With D_{im} equal to the largest dimension of the antenna aperture. The distance between the antennas should be large compared to the wavelength ($\approx$ 10x) and dimension of the antenna to ensure that the radiated waves will behave as planar waves. This also means that the boundary for far-field operation will be different for a very large antenna compared to an electrically small antenna.

On-chip antennas: more substrate, more problems

From Equation 3.9, the received power can be increased by implementing antennas with higher gain. Since antenna size depends on the wavelength at the operating frequency, antennas for MHz/GHz applications tend to be large: a free-space halve wavelength dipole antenna at 300MHz would be 50cm long, whereas at 60GHz it would still be 2.5mm long in addition to the space around it. Consequently, this would take a lot of expensive silicon area if implemented on-chip, and thus antennas for these types of circuits are mainly positioned off-chip. For THz signals, however, the dimensions of the antennas become small enough that the area usage for on-chip antennas becomes manageable. Off-chip antennas could still be an option, as their larger size and wide array of design choices results in a higher directivity and efficiency. However, as mentioned in Section 3.1, getting the THz signals off-chip and transported to the off-chip antenna becomes a difficult and potentially lossy endeavor.

When designing on-chip antennas for THz radiation, the substrate will have a large impact on the performance of the antenna (Figure 3.6). For a CMOS technology, the low-resistivity silicon substrate ($\approx 10\Omega - cm$) and the high dielectric constant ($\varepsilon_r = 11.9$) is the main culprit for the lower radiation efficiency compared to off-chip antennas. Besides having a radiation component upwards in the air, a significant amount of power will propagate through the substrate and be radiated on the backside of the silicon wafer.

The first loss contributor are the conductive losses in the substrate, similar to the substrate losses of on-chip passives at high frequency (Section 2.3). Increasing the

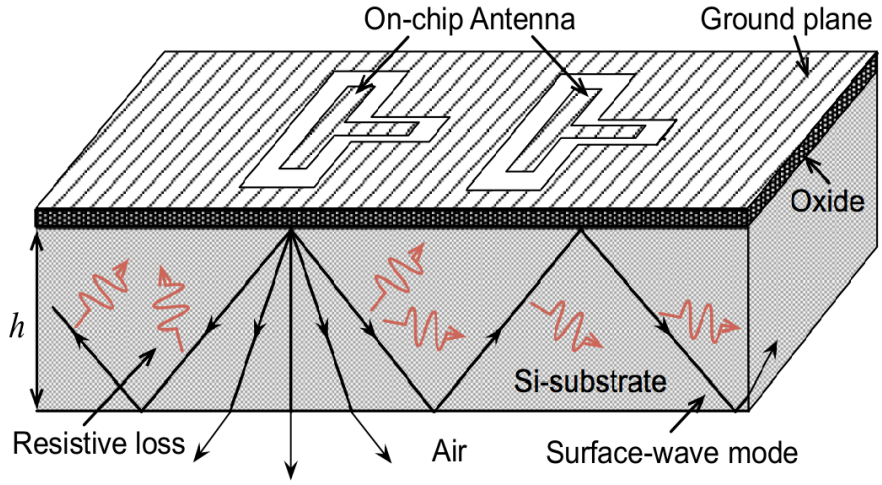


Figure 3.6: Illustration of the substrate radiation problem in a silicon chip, where a substantial part of the radiation is trapped in the substrate due to surface waves and being radiated through the (back)side of the chip [Par13]

substrate resistivity can be achieved by moving to an SOI process technology or additional process steps, but this will come at an significant increase in production cost.

The second loss mechanism is due to the high substrate permittivity and the excitation of surface waves. While a more in-depth discussion on higher-order surface modes would be beyond the scope of this work, a brief introduction of the matter is given for the reader's general understanding. Because of the silicon substrate's high permittivity, the substrate will effectively be a dielectric slab waveguide where the antenna will couple to higher-order surface waves depending on the substrate thickness. From [Poz83], an expression for the cut-off frequency of higher-order surface waves in a grounded dielectric slab can be given:

$$f_c = \frac{n \cdot c}{4 \cdot d\sqrt{\varepsilon_r - 1}} \tag{3.12}$$

In Equation 3.12, f_c is the cut-off frequency and n the surface wave mode. The TM_0 wave has no cut-off frequency, and can thus be excited for any substrate thickness. A portion of the substrate wave power will be dissipated in the silicon substrate as a loss, and the remaining power will be radiated from the sides of the substrate in an unwanted direction, reducing the antenna directivity. Reducing the relative permittivity would increase the frequency at which the first surface wave (TE_1) could be excited, but this

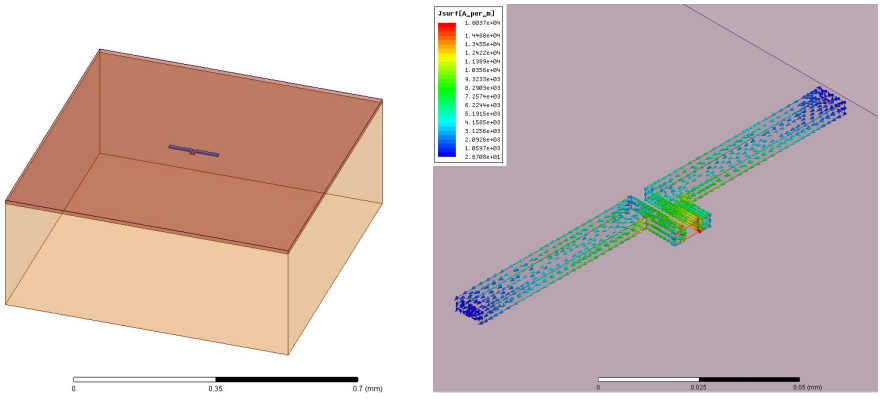
would require a different substrate (PTFE, $\varepsilon_r = 2.17$) and is not an option in the CMOS process. By reducing the substrate thickness, the number of higher-order substrate modes that the antenna can couple to can be reduced and the efficiency of the on-chip antenna increased. This can be done by applying a wafer thinning process step to the chip [Sen12]. However, to truly reduce the losses due to surface waves, the silicon substrate should be thinned to less than $0.01\lambda_0$ for a dipole antenna [Ale83]. At THz frequencies, with its sub-mm wavelengths, this would result in impractical thicknesses and mechanically frail substrates. Therefore, wafer thinning is not utilized in this work, and the silicon substrate of all chips, unless specified otherwise, is a foundry-standard 12 mils ($\approx 300\mu$m).

In summary, the majority of problems associated with on-chip antennas is due to the lossy, high permittivity substrate and unwanted coupling of radiation waves into substrate waves and backside radiation. To quantify the impact of these issues, we will illustrate some of the difficulties and problems of on-chip antennas using several examples in the next section.

3.3.3 On-chip half-wave dipole antenna

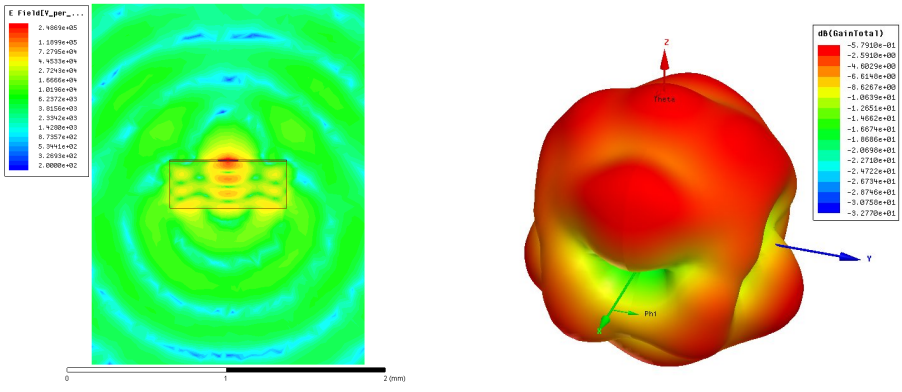
The dipole antenna is the most basic and common antenna type. It was first used and described by Heinrich Hertz in 1886, and is the first type of antenna ever invented [Her87]. It consists of two in-line conducting rods, which are fed by a source in between the two antenna rods or legs. The two halves of the antenna will form a resonator at a frequency determined by the length of the antenna. Consequently, the target frequency and corresponding wavelength λ determine the dimension of the dipole antenna. The most common dipole antenna is a half-wave dipole, where each antenna rod is a quarter wavelength of the target frequency. The rods are positioned symmetrically and fed in the middle of the antenna.

An ideal half-wave dipole suspended in air will have a radiation pattern that is close to being omnidirectional. Since fully omnidirectional antennas are not physically possible (Section 3.3.1), the radiation pattern looks like a toroid or donut, where the radiation drops to zero along the antenna's axis. The directivity of a dipole is therefore relatively low, with the ideal free-space half-wave dipole having a peak directivity of 2.15dBi. A free-space dipole simulation model, radiation pattern and E-field distribution have been included in Appendix B.2. Since the dipole antenna is so common, it is also used as a reference antenna just like the isotropic antenna (with the difference that a dipole antenna is not a theoretical concept). Antenna directivity and gain using the dipole as a reference are indicated by decibel-dipole (dBd), where a gain of 0dBd is equal to a gain of 2.15dBi. As mentioned earlier, this work refers antenna properties to that of an isotropic radiator. Therefore, dBi and dB will be used interchangeably unless stated otherwise.



(a) (b)

Figure 3.7: 3D simulation model (a) and current distribution (b) in an on-chip dipole antenna at 540GHz



(a) (b)

Figure 3.8: E-field (a) and radiation pattern (gain, dB) (b) of the on-chip dipole antenna. The surface waves are visible in the silicon substrate

With increasing frequency, the wavelength and corresponding size of a half-wave dipole becomes small enough to effectively be implemented on-chip. The half-wave dipole antenna with a length of 130μm dimensioned to resonate at 0.54THz, and the silicon substrate are shown in Figure 3.7a. A close-up of the antenna, as well as the current distribution in the antenna's branches is given in Figure 3.7b. The current distribution forms a standing wave, which reaches its peak at the center and has a node at both ends of the dipole.

In Figure 3.8b, the 3D radiation pattern (gain) is shown for radiation at 0.54THz. The simulated peak directivity is 4.1dB for the front side (positive Z direction) and 3.67dB for the backside lobe (negative Z direction, through the substrate). With a simulated radiation efficiency η_{rad} equal to 30.9%, the resulting antenna gain is -1.02dB front side and -1.4dB back side. When integrating the antenna in a system, the antenna impedance should be matched with the output impedance of the circuit block connected to it. Failing to do so will result in reflection losses due to mismatch, and will reduce the amount of power being accepted by the antenna to be converted in radiated power. Since both antenna and circuit impedance vary over frequency, there will be a limited bandwidth where the antenna is matched and will operate effectively. This bandwidth is commonly taken as the frequency range where the S11 or reflection coefficient Γ of the antenna is below -10dB. The antenna bandwidth can be specified as an absolute bandwidth (BW) or a fractional bandwidth (FBW):

$$FBW_{\%} = \frac{f_{high} - f_{low}}{f_{center}} \cdot 100 \tag{3.13}$$

For the on-chip dipole of Figure 3.7a, the center frequency is 0.54THz with Γ equal to -25dB (Figure 3.9). The -10dB reflection coefficient ranges from 502-562GHz, resulting in a bandwidth of 60 GHz or a fractional bandwidth of 11.1%. A large BW is preferred, as this allows a wider range of frequencies that can effectively use the antenna. In addition, this makes the whole radiating system more robust for any process variations that can change the center frequency of the circuit.

One of the main issues with integrating antennas on-chip is the presence of the high permittivity silicon substrate and the resulting conductive losses and possible excited surface wave modes. The presence of these substrate waves and radiated energy into the substrate is visible in Figure 3.8a, where the substrate is a foundry-standard 300μm thick. To quantify the impact of the substrate on the radiation efficiency, the silicon substrate thickness was swept and the resulting η_{rad} plotted in Figure 3.10. The simulated efficiency figures confirm that thinner substrates have higher radiation efficiency due to less higher-order substrate modes being excited (Equation 3.12), which can be achieved by applying wafer-thinning post-process steps. For increasing substrate thickness, the power of the different possible modes can rise or fall, which results in a seemingly oscillating η_{rad} for varying substrate thickness [Ale83].

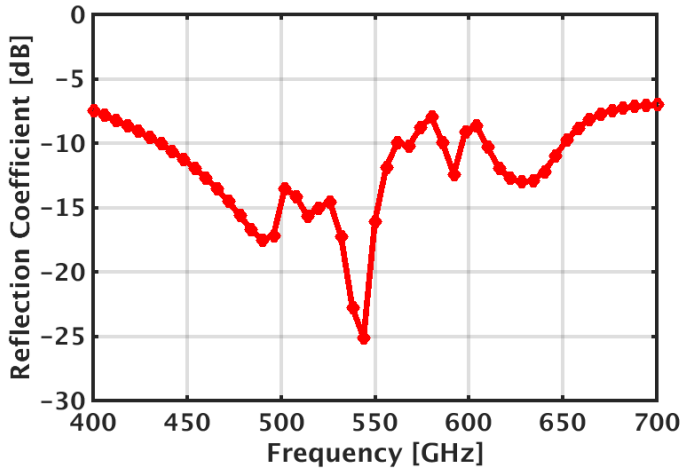


Figure 3.9: Simulated eflection coefficient of an on-chip dipole with center frequency 0.54THz.

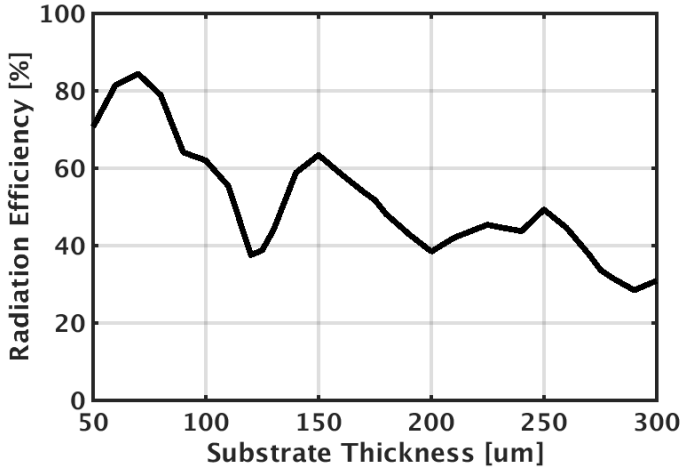


Figure 3.10: Simulated radiation efficiency of a 0.54THz on-chip dipole antenna for an increasing silicon substrate thickness, demonstrating the increasing losses due to higher-order surface waves in thicker substrate materials

There are many variations and possible adaptions to improve the antenna performance of an on-chip dipole antenna, which will be covered later in the relevant chapters.

3.3.4 On-chip square patch antenna

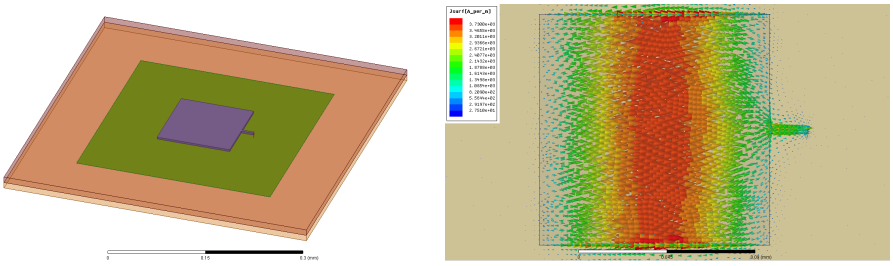
A more directive antenna than the dipole, and one that is also compatible with CMOS chip design, is the patch antenna or microstrip antenna, first described in 1972 by John Howell [How72]. The patch antenna exists of a rectangular patch and a reflecting ground plane implemented in a conducting material. Figure 3.11a shows the 3D model of a rectangular patch antenna implemented in the top (patch) and bottom (ground plane) metal of a CMOS process. Together they will form a resonating microstrip transmission line, where the effective length is equal to half a wavelength of the radiated signal. The patch antenna center frequency can be approximated by:

$$f_{patch} = 0.49 \cdot \frac{c}{L_{patch} \cdot \sqrt{\varepsilon_r}} \tag{3.14}$$

Due to the fringing fields at the edges of the patch, the electrical size of the patch is a little larger than the physical dimensions. This results in a patch length of 0.49 times the wavelength instead of half. The width of the antenna will determine the antenna impedance and can be used to match the patch impedance to that of the rest of the circuit. The patch antenna in Figure 3.11 is a square patch with a length of 115µm, targeting a radiation frequency of 0.6THz. Figure 3.11b shows the current distribution in the patch: the current is maximal at the center of the patch's length, and reduces to zero at both edges. The voltage follows an inverse pattern, with peak values at the edges and reaching zero in the middle of the patch. This virtual ground, where the impedance is theoretically equal to zero Ω, could be used for DC biasing of the antenna. The antenna impedance rises when approaching the patch edge, to reach its peak value at the edge, usually equal to several hundred Ω.

Since the large ground plane shields the silicon substrate from the patch antenna, the total height of the simulation model can be reduced to 10µm instead of 310µm. This drastically reduces the total volume of the simulation model and the corresponding EM-simulation time. The E-fields of the on-chip patch antenna are given in Figure 3.12. The back-side radiation is drastically reduced due to the ground plane, resulting in a main radiation lobe in the front-side direction. The extending electric field beyond the physical dimensions of the patch can be noticed, and it is this fringing field that causes the patch antenna to radiate.

The simulated radiation pattern (gain) is plotted in Figure 3.13. The peak directivity is 6.35dB, η_{rad} is 36.1 % and the resulting peak gain is 1.97dB for a center frequency of 0.6THz. The front-to-back side ratio is very large thanks to the ground plane. In



(a) (b)

Figure 3.11: 3D simulation model (a) and current distribution (b) in a 115µm x 115µm on-chip patch antenna at 600GHz

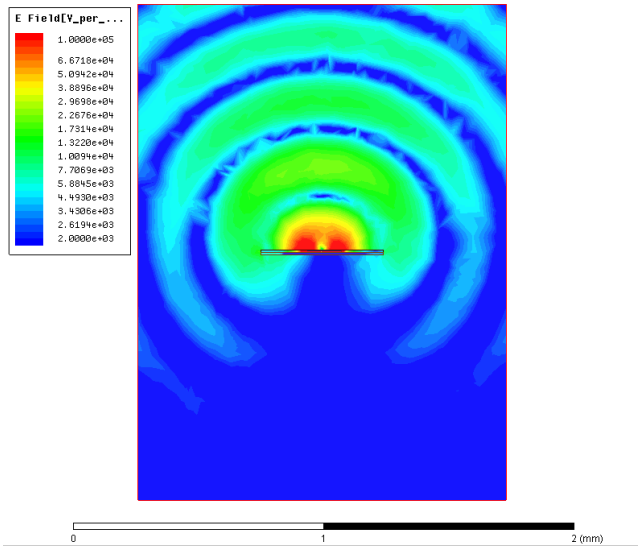


Figure 3.12: E-fields of the on-chip patch antenna, showing a large fron-side to back-side radiation ratio

a regularly mounted and wirebonded chip die, this directive front-side lobe is a very convenient property of the on-chip patch antenna. However, one of the major downsides of using a patch antenna is its narrow bandwidth: the bandwidth of this patch antenna ranges from 592.16-607.3GHz, resulting in an absolute BW of 15.4GHz or a FBW of 2.56%. Considering that process variations and modeling inaccuracy can easily vary the operating frequency by several tens of GHz, the usage of patch antennas can be considered if the frequency tuning range of the system can compensate any shifts in

center frequency. The classical patch antenna described here is a single-ended antenna, but could be modified to a differential version if required.

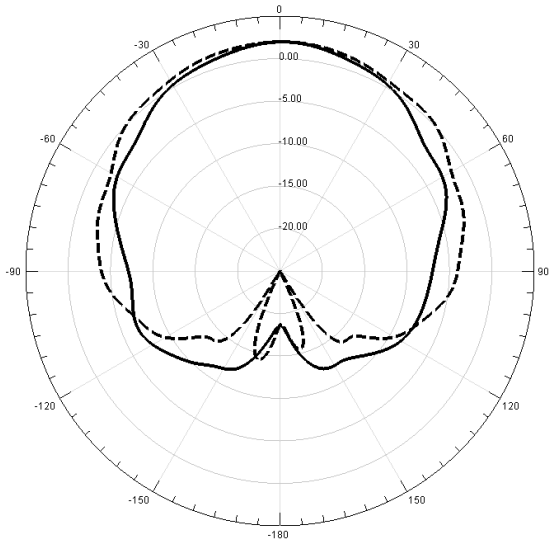


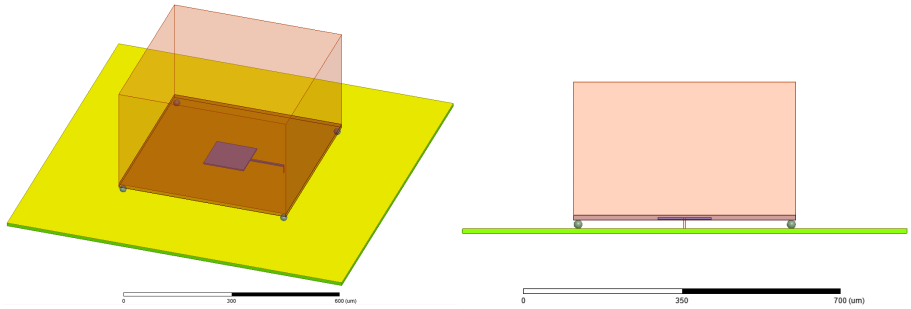
Figure 3.13: Radiation pattern (gain) of the on-chip patch antenna at 600GHz (ϕ angle: dashed = 0°, solid = 90°)

3.3.5 Flip-Chip Patch Antenna for improved BW

While the patch antenna has a higher directivity than the dipole antenna, the narrow bandwidth could possibly render it useless when the center frequency of the circuit changes. The patch bandwidth is determined by the dielectric height or distance between the patch and ground plane: the patch and ground plane form a leaky-cavity resonator, and the closer the two are together, the higher the quality factor of this cavity becomes, reducing the bandwidth. Increasing the distance between patch and ground plane would thus increase this bandwidth.

When implemented in a CMOS process, the distance between patch and ground plane is very small compared to the wavelength. When using both top and bottom metal, the spacing will be in the order of several μm. To increase the patch antenna bandwidth while maintaining the directive radiation pattern and large front-side to back-side lobe ratio, a "flipped patch" antenna is proposed (Figure 3.14). In this topology, the patch is implemented on-chip, while the metal ground plane is placed on a carrier PCB. The silicon die is than flip-chipped, so that the distance between the patch and ground

plane is determined by the ball height of the golden ball studs used in the flip-chip bonding process (Section 3.1). The increased patch-ground plane distance reduces the resonating cavity quality factor, which results in a larger antenna bandwidth.



(a) (b)

Figure 3.14: 3D model (a) and side view (b) of the flipped on-chip patch antenna

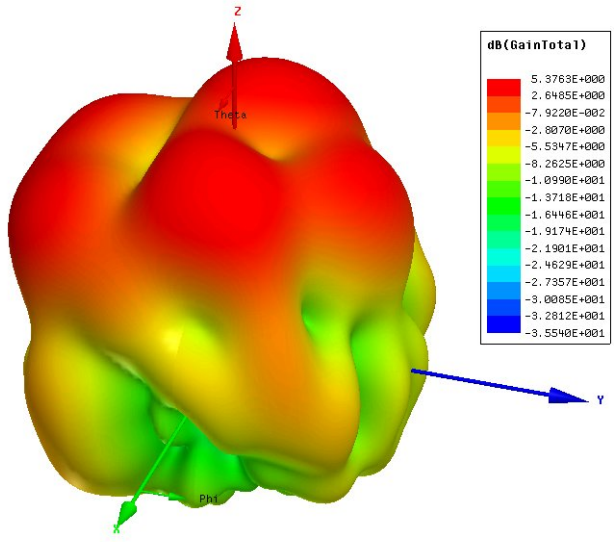


Figure 3.15: 3D radiation pattern (gain) of the flipped on-chip patch antenna with off-chip ground plane, radiating at 600GHz

The 3D radiation pattern of the flipped patch antenna is shown in Figure 3.15. The main radiation lobe is through the silicon substrate (E-fields are shown in Appendix B.3), which in turn excites surface waves in the substrate. The simulated peak directivity of this flipped patch antenna is 9.36dB, a η_{rad} of 40% and a peak gain of 5.38dB. The increased directivity is due to the silicon substrate, which functions as a rectangular dielectric lens.

In Figure 3.16, the reflection coefficient is plotted for both the on-chip patch antenna from Section 3.3.4 and the flipped patch antenna from Figure 3.14. Both were designed to have a center frequency at 600Ghz and achieve a S11 below -25dB at the target frequency. The improvement in bandwidth of the flipped patch compared to the regular narrowband patch is very clear from this figure: the flipped patch antenna has a bandwidth ranging from 545.6-630.9GHz. The resulting 85.3GHz absolute BW and 14.2% FBW of the flipped patch are a 5.5 times improvement in bandwidth compared to the regular patch antenna.

The proposed flipped patch antenna demonstrates that the limited bandwidth of the on-chip patch antenna can be enhanced by modifying the distance between the on-chip patch and the on-board ground plane using the flip-chip bonding and mounting techniques. The nominal height of the flip-chip ball studs is approximately 20μm, but larger or multiple, stacked gold studs could be used to further increase the patch-ground plane spacing. By attaching a lens on the backside of the substrate, the antenna directivity could be even improved further.

3.4 Lenses and off-chip antennas

Besides the different on-chip antenna types, off-chip components or packaging techniques can be used to alleviate some of the performance limiters of on-chip antennas. In addition, off-chip antennas suffer much less from the on-chip performance constraints, and can take larger dimensions. These options often require extra packaging steps and come at significant additional costs, but can be justified depending on the application and performance requirements.

3.4.1 Substrate Lenses

The surface wave problems due to the high permittivity of the substrate can be contained by using a silicon lens. Figure 3.17 depicts an on-chip dipole on a standard silicon substrate, augmented with a silicon lens on the substrate side. This "substrate lens" will eliminate the substrate wave problem: the antenna will radiate the majority of its power into the substrate (a factor of ε_r for a dipole antenna) [Reb92], and the lens' shape

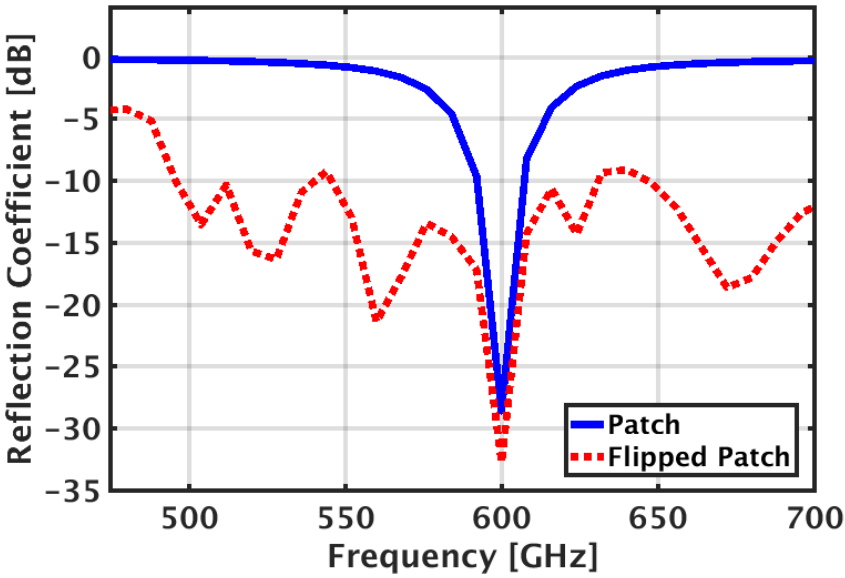


Figure 3.16: Reflection coefficients (S11) of a regular on-chip patch antenna (solid) and a flipped patch antenna (dash) designed at 0.6THz

will ensure that no waves will be internally reflected and become a trapped surface wave. Most of the power radiated into the substrate by the antenna will be radiated to the air on the backside due to the substrate lens (Figure 3.18), drastically improving both efficiency and directivity. The radiation pattern is given in Figure 3.19 where directivity and efficiency is greatly improved compared to the stand-alone on-chip dipole of Figure 3.7. While the advantages are numerous, the large additional cost of the substrate lens and increased complexity of the packaging process would limit the usage of silicon substrate lenses to academic research and niche markets. In the author's opinion, the hugely disproportional cost of adding a substrate lens is currently irreconcilable with the fundamental argument for using CMOS (extreme low-cost, mass-production compatible), and will thus not be used in this work.

Several lens types are available and successfully used to improve the radiation properties of THz chips: hemispherical, hypo-spherical and extended hemispherical ("bullet") dielectric lenses can be used, depending on the position of the source in relation to the focus point of these lenses. In an extended hemispherical lens for example, the length of the straight dielectric extension can be used to synthesize an elliptical lens with the focus point that incorporates the substrate thickness of the silicon chip, without the

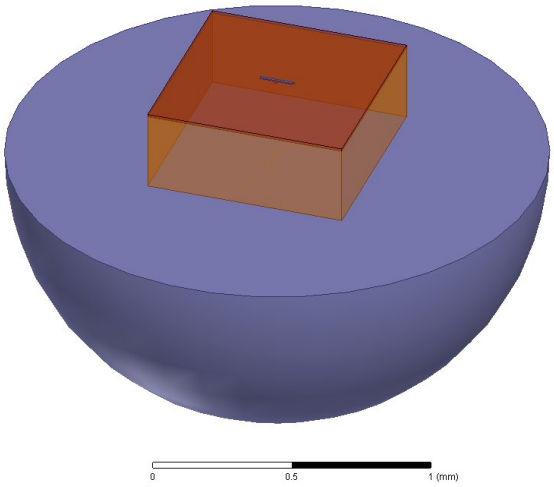


Figure 3.17: Simulation model of a on-chip dipole antenna mounted on a silicon lens

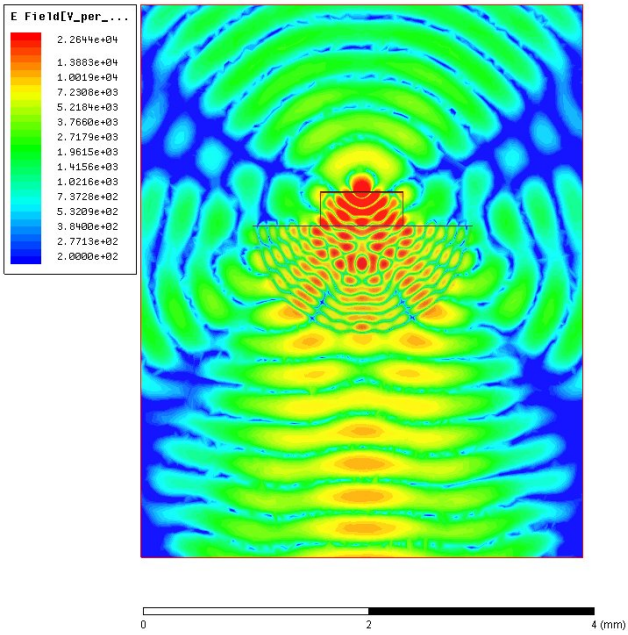


Figure 3.18: Electric fields present in a on-chip dipole antenna mounted on a silicon lens

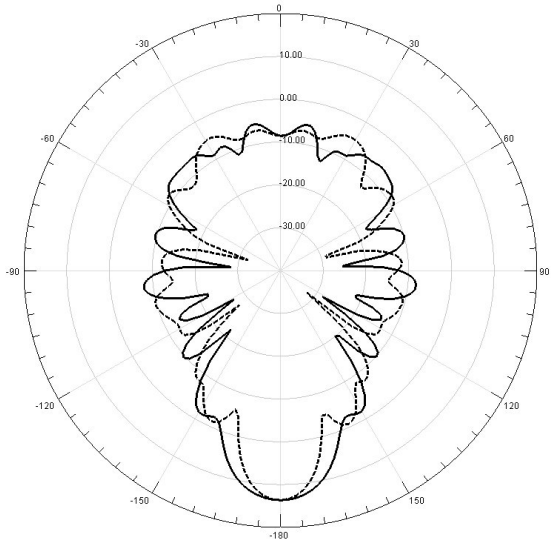


Figure 3.19: Radiation pattern (gain, dB) of a silicon lens-mounted dipole antenna (ϕ angle: dashed = 0°, solid = 90°)

need for wafer thinning [Fil93]. Antenna directivity up to 30dB have been reported at 550GHz using a hemispherical silicon substrate lens [Pfe14].

3D printed lenses

Great improvements have been made in the field of 3D printing, which has improved the availability and the attainable resolution of the technology. An interesting approach would be to 3D print lenses on top of the silicon die, or to make custom shaped lenses that better fit the transmitter/receiver requirements. Several polymers are a potential candidate to fill in this role, and their dielectric properties in the THz range can be found in Table 3.4.1. While all materials have a similar refractive index n, large differences in absorption in the THz region can be distinguished. The commonly used materials for consumer 3D printing, ABS and PLA, both have significant absorption losses at THz frequency. Their availability and low cost are strong advantages, but the high loss tangent would only tolerate very thin lenses before any gain in antenna performance is offset by the material losses. Both HDPE and PP have very low absorption losses over the whole THz frequency range, as well as a relatively stable refractive index over a wide range of frequencies. These advantageous properties would make HDPE and PP strong candidates for THz lens materials. Unfortunately, the 3D printing qualities of HDPE and PP are lower than ABS and PLA, which explains the latter's popularity

Material	Refr. index n	$tan\delta$ / abs. coeff. (cm^{-1})	Freq.	ref.
SU-8	1.7	0.075	1THz	[Gha15]
SU-8	1.7	0.06	500GHz	[Gha15]
ABS	1.57	5 cm^{-1}	500GHz	[Bus14]
ABS	1.65	0.05/ 18cm^{-1}	1THz	[Jin06]
PLA	1.89	11	500GHz	[Bus14]
HDPE	1.53	0.002	1THz	[Hej11]
PP	1.51	0.002	1THz	[Hej11]
InP	3.5	0.009	1THz	[Hej11]
PS	1.56	0.5cm^{-1}	500GHz	[Bus14]

Table 3.1: Table with the dielectric properties at 1THz for 3D printable dielectrics

in the 3D printing community. PTFE, more commonly known as Teflon, is another polymer that shares very similar characteristics as HDPE and PP and is already being used in some commercial laboratory lenses [Tho17] rated for 500GHz and higher.

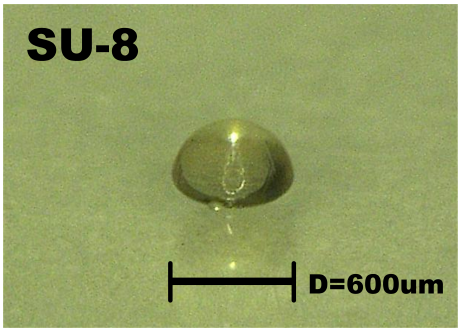
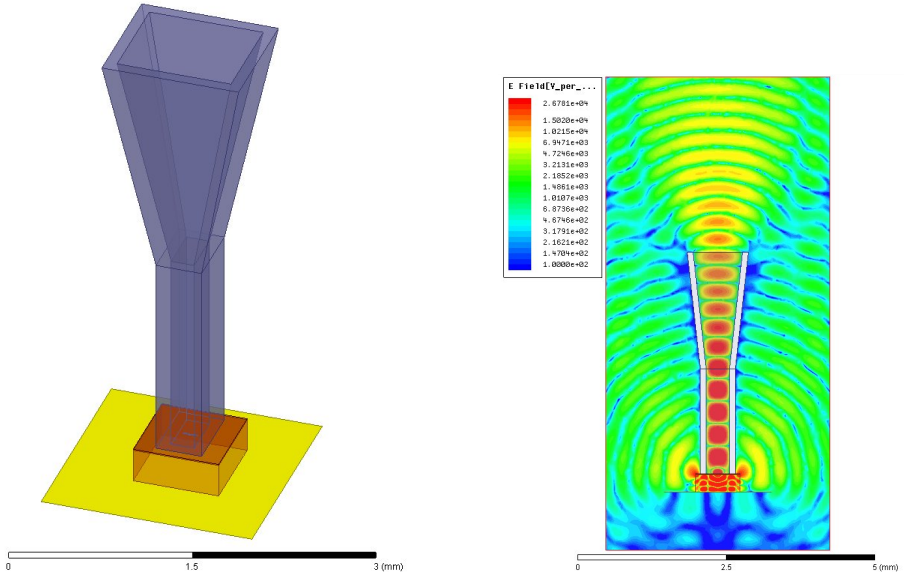


Figure 3.20: 3D-printed lens with a diameter of 600µm using SU-8 photoresist

An interesting material that has a loss tangent positioned between HDPE and ABS is SU-8, a type of photoresist. By using a focused laser beam, very accurate lenses and other dielectric structures can be "printed" using SU-8 with a resolution of µm. Figure 3.20 shows a hemispherical lens with a diameter of 600µm that was created using the SU-8 photoresist. The small size of the lens allows it to be placed on top of a chip, directly on top of the on-chip antenna and located between the bondwires. The dielectric lens improves the front-side radiation pattern of the radiator while maintaining a compact form factor. Alternatively, other shapes and structures can also easily be created using SU-8 and other printable materials, allowing the on-wafer integration of radiation-improving structures.



(a) (b)

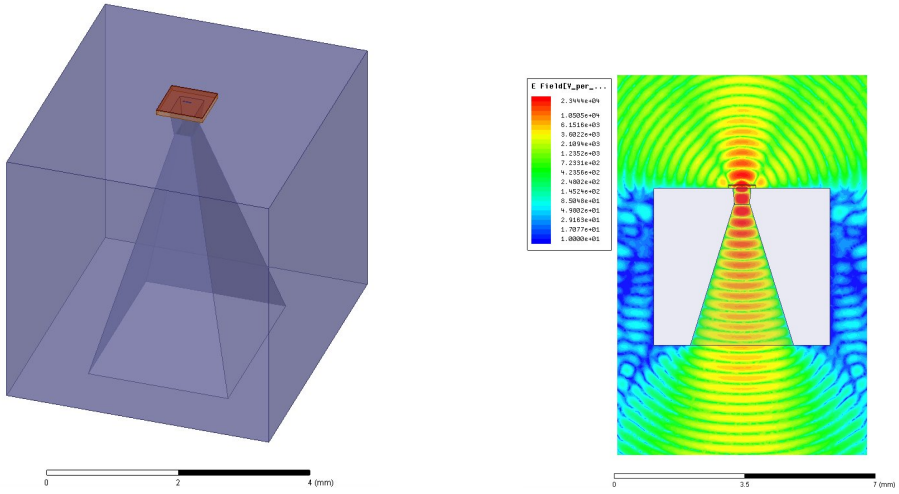
Figure 3.21: Metal-coated horn antenna mounted on top of a 0.54THz signal generator with on-chip dipole

3.4.2 Off-chip antennas

Even if they require a more complex packaging process and come at an additional cost, off-chip antennas remain an efficient and performing solution for THz radiation purposes.

Full-fledged off-chip antennas can be fabricated and have been demonstrated at 300GHz [Kaw15] with a complete packaged system, where the signal-generating chip is flip-chipped onto a board with microstrip line connecting the chip with a metal horn antenna. The improvement in antenna efficiency and directivity from off-chip antennas is somewhat offset by the non-trivial task of getting the THz signals off-chip, as demonstrated in the first sections of this chapter.

Figure 3.21 shows the model and E-fields of a 3D printable and metal-coated horn antenna, which could be mounted on top of the silicon wafer. The horn antenna follows the classical horn antenna design used by larger off-chip variants that are frequently used in measurement systems. The on-chip signal generator would launch the 0.54THz signal into the waveguide part of the horn antenna through an on-chip antenna or other coupling mechanism. The peak gain realized by this structure is 9.7dB and the corresponding radiation patterns are included in Appendix B.4. Another possible



(a) (b)

Figure 3.22: Metal-coated horn antenna added to the back side of the wafer-thinned 0.54THz signal generator chip with on-chip dipole antenna

external antenna solution is shown in Figure 3.22, where a 3D printable and metal-coated horn antenna is placed at the backside of the silicon substrate. To improve the coupling of the 0.54THz signal into the backside antenna, the silicon substrate of the chip is thinned to 75µm. As the dimensions of the horn antenna become small at sub-mm wave frequencies, the space around the horn antenna is filled to provide mechanical stability to the structure, as well as provide a mounting surface for the chip. The radiation pattern is included in Appendix B.4 and shows that achieved gain of the main radiation lobe is almost 14dB.

Another approach is to fabricate pseudo-integrated antennas, thereby bypassing the substrate-surface wave problem: by arranging the bondwires on top of the silicon wafer in a particular fashion, radiating structures can be implemented [Ma13]. These bondwire antennas have been successfully demonstrated at frequencies up to 120GHz [Def14], but require precise packaging steps and extra care not to damage the fragile bond wire positions.

3.5 Conclusions on antennas

In this chapter, an overview of the different possible techniques to get THz signals off-chip have been given and analyzed. While both bondwires and flip-chip could be used

to transfer THz signals from the on-chip generator circuit to an off-chip board, their delicate matching needs and hard practical fabrication limitations are major roadblocks. High-frequency probes are an essential tool when wanting to characterize the on-wafer performance of integrated circuits with high accuracy in a well-controlled environment. Nevertheless, their fragile nature and advanced measurement setup requirements limits their use to measurement labs in both academia and industrial research centers.

With the alternative options lacking in performance or flexibility, and the wavelength being reduced enough to enable fully integrated implementation, on-chip antennas are becoming an important part of THz integrated electronics. In this chapter, the main issues associated with on-chip antennas, several antenna types and various packaging options and solutions have been discussed. Depending on the application, available technology and project cost, the designer can choose a radiating solution fitting their needs. In the rest of this work, as far as on-chip antennas is concerned, the focus will be on lens-free radiating solutions with a minimal of additional packaging requirements. This low-cost, mass-production compatible approach is consistent with the usage of CMOS technology throughout this work.

As the system complexity of THz communication and imaging systems increases, so will the importance of fully integrated antennas. Although there is plenty of crucial and interesting research efforts remaining on the topic of THz antennas, this work's main focus is on the implementation of THz integrated circuits. As such, a more hands-on approach towards antennas is applied and the resulting on-chip antennas are the initial endeavors into the vast and fascinating field of THz radiation.

Chapter 4

THz transmitter circuits

Oscillator circuits are a fundamental building block responsible for the generation of an AC signal at the target frequency. In this chapter, we will discuss the requirements for oscillation, performance indicators and the usage of harmonics to generate THz signals beyond the f_{max} limitation of CMOS technology. The theory and conclusions from Chapter 2 and Chapter 3 will be applied in the design of several THz transmitters in deep-scale nanometer CMOS technologies. Measurement results and THz imaging experiments will be discussed and analyzed, demonstrating the feasibility of integrated THz radiators in CMOS technology.

4.1 Oscillator concepts and topologies

As oscillators are such an important component in many electronic systems, there are several design parameters that should be considered when evaluating their performance. The oscillation frequency will be the most obvious design parameter, followed by the output power which is usually expressed in dBm. The oscillation frequency should also be controllable over a wide frequency range, called the tuning range. Oscillators whose frequency can be tuned by changing a control voltage, are called voltage-controlled oscillators (VCO). DC power consumption, 3-dB bandwidth, phase noise and many more performance indicators are all part of the considerations that should be taken when designing oscillators, and will be explained and discussed in the following sections.

4.1.1 Barkhausen stability criterion

One of the most common models to represent an oscillating system is based on an amplifier system with a feedback loop, as shown in Figure 4.1. The transfer function of the closed-loop system can be written as:

$$H(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{A(j\omega)}{1 - A(j\omega) \cdot \beta(j\omega)} \tag{4.1}$$

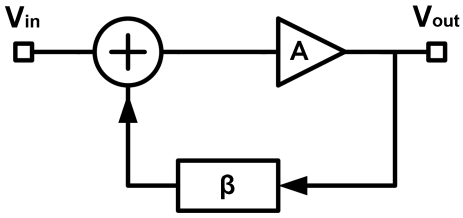


Figure 4.1: Schematic showing the feedback system representing the oscillator behavior

With $A(j\omega)$ the amplifier gain and $\beta(j\omega)$ the transfer function of the feedback network, both as a function of frequency ω. To achieve steady-state oscillation, the Barkhausen criteria should be met in this feedback system at the target frequency ω_{osc}, which are as follows:

$$|A(j\omega_{osc}) \cdot \beta(j\omega_{osc})| = 1 \tag{4.2}$$

$$\angle A(j\omega_{osc}) \cdot \beta(j\omega_{osc}) = n \cdot 360°; n \in 0, 1, 2, 3, \ldots \tag{4.3}$$

Initially, there is no oscillation in the system. Oscillation is started by a sharp input waveform, an initial condition of the system or the presence of noise which is amplified and fed back in the loop. If the loop gain is larger than unity, the oscillation amplitude will continue to rise. As the feedback system depends on both frequency and oscillation amplitude, the oscillation will reach a steady-state or stable oscillation when the loop gain is unity (Equation 4.2) and the total phase shift is a multiple of 360° (Equation 4.3) at the oscillation frequency ω_{osc} with the oscillation amplitude V_{osc}. From these criteria, we can already define a fundamental requirement for high-frequency oscillator circuits: the highest stable oscillation frequency achievable by the feedback system is the maximum frequency where unity gain can be maintained by the circuit.

4.1.2 LC tank losses and negative-resistance oscillator model

Another, more intuitive way of representing an oscillator system is the negative-resistance model, depicted in Figure 4.2. In this case, LC forms the resonator, and R_p is the losses of the tank. In an ideal resonator tank, R would be zero and the tank would periodically exchange its energy between the L_p and C_p, keeping the oscillation going

forever. The real, non-ideal tank has a non-zero resistive loss component R_p, which dissipates a part of the resonator energy during each cycle, damping the oscillation until it completely stops. By adding a negative resistance generator circuit (NRGC), for example an active circuit or diode, the R_p tank loss can be compensated, allowing steady-state oscillation in the resonator tank. The requirement for this negative-resistance is that it is larger than the tank loss at start-up, and becomes equal to unity to achieve stable oscillation.

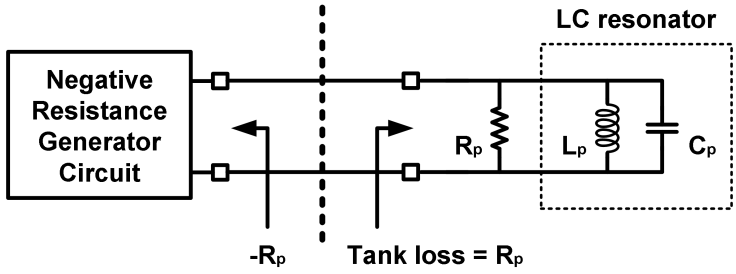


Figure 4.2: Negative-resistance equivalent model of the oscillator tank, and the active circuit required to compensate the tank loss

$$|R_{NRGC}(start-up)| > R_p(\omega_{osc}) \tag{4.4}$$

$$R_p(\omega_{osc}) + R_{NRGC}(\omega_{osc}) = 0 \tag{4.5}$$

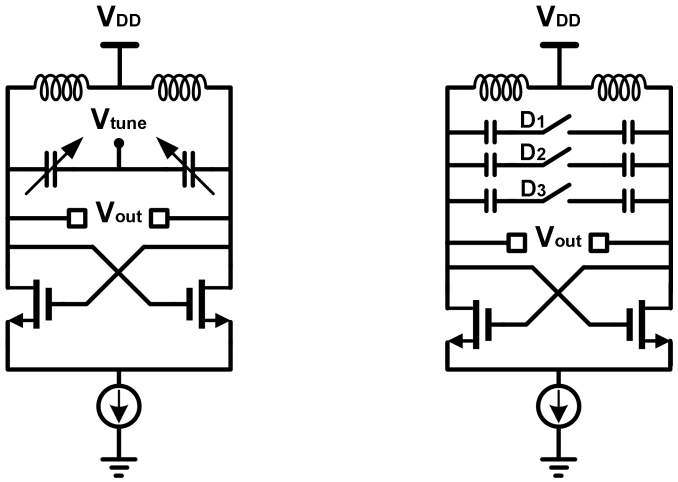
As was discussed in Section 2.3, this R_p component will determine the quality factor Q of the resonator tank, which depends on both the inductor and capacitor quality factor (Equation 4.6). High-Q tanks will therefore require less negative-resistance compensation of the tank losses compared to low-Q resonators, and will therefore oscillate more easily and more efficiently.

$$\frac{1}{Q_{Tank}} = \frac{1}{Q_{Ind}} + \frac{1}{Q_{Cap}} \tag{4.6}$$

4.1.3 VCO topologies

While a variety of different VCO topologies exist, the most popular topology is the cross-coupled oscillator topology, shown in Figure 4.3. One of the first CMOS implementations of this topology was presented in [Cra95] and has been the go-to

oscillator topology for RF and high-frequency oscillators ever since, and has reached fundamental oscillation frequencies as high as 300GHz [Raz11].



(a) (b)

Figure 4.3: Schematics of the classical cross-coupled VCO topology (a) and the DCO variant (b) with digitally controllable capacitor bank

The oscillation frequency (Equation 4.7) is determined by an inductor L and the total capacitance comprising of a fixed capacitance C and a variable capacitance C_{var} which can be used to tune the oscillation frequency. For continuous tuning, this variable capacitance can be implemented by varactors [Bun03] (Figure 4.3a). For discrete frequency steps, a capacitor bank with digitally controllable switches can be used (Figure 4.3b), more commonly referred to as a digitally-controlled oscillator (DCO).

$$f_{osc} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot (C + C_{Var})}} \tag{4.7}$$

As mentioned in Section 4.1.2, a negative resistance generated by an active circuit should be added to the LC tank to compensate any tank losses. In a cross-coupled VCO, this is achieved by connecting the drain of one transistor to the gate of the other. By connecting the transistors in this way, the cross-coupled pair generates a differential impedance equal to -2/gm (Figure 4.4). The parasitic capacitance of the transistors is added to the total capacitance of the tank, and this will also influence the oscillation frequency. Without the cross-coupled pair, any oscillation of the LC tank will be damped by the resistive component and will eventually die out. The negative resistance

created by the cross-coupled transistor pair will compensate for this resistive loss, and as a result constant oscillation can be maintained.

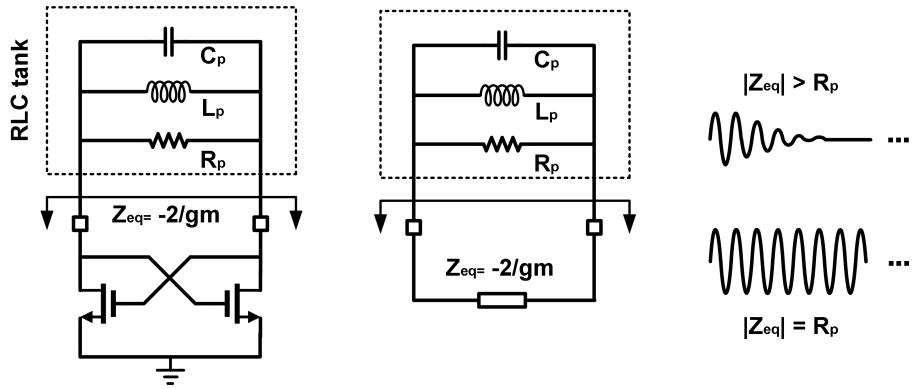


Figure 4.4: A cross-coupled transistor pair (left) and equivalent negative-resistance (middle) to compensate the tank losses. Depending on *gm*, this will result in decaying or sustained oscillation (right)

From Equation 4.4 we can conclude that the *gm* of the cross-coupled transistors should be large enough at oscillation start-up to grow the oscillation amplitude at the target frequency. To reach steady-state oscillation, Equation 4.5 states that the negative resistance of the cross-coupled pair should be equal to the total tank loss at the target frequency. While the -2/*gm* value of the cross-coupled pair is a good approximation at lower frequencies, it ignores the influence of the transistors' gate resistance R_g, the gate-source capacitor C_{gs} and gate-drain capacitors C_{gd} at high frequency. The resulting admittance acquires some frequency-dependent components and can be written as [Raz11]:

$$Y_{cross-coupled}(s) = \frac{-gm + R_g C_{gs} C_{gd} s^2 + [C_{gs} + (4 + gmR_g) C_{gd}] s}{2[R_g (C_{gs} + C_{gd}) s + 1]} \tag{4.8}$$

By taking the real and imaginary parts of Equation 4.8, we find that the equivalent model of the cross-coupled transistor pair comprises of the negative resistance -2/*gm* in parallel with several frequency-dependent positive resistances and capacitors. These additional components will counter the negative resistance generation at high frequencies, and will prevent the cross-coupled pair from sufficiently compensating the LC tank losses and achieve stable oscillation.

Another perspective on the oscillator frequency limit is that the active circuit should have enough power gain at the target frequency to be able to compensate the power

being dissipated due to tank losses. This proves to be a fundamental problem when going towards THz oscillators: there is no gain above f_{max}. Since a loop gain of 1 is a requirement for stable oscillation as per the Barkhausen criterion, no fundamental oscillation can be maintained above the f_{max}. In practice, this maximum frequency ω_0 will drop even further, as the f_{max} limitation assumes a perfectly lossless interconnect network with perfect input and output matching of the transistors. Because of design margins taken to accommodate model inaccuracies, mismatch, interconnection losses and to ensure oscillation start-up, the actual oscillation frequency ω_0 will always be tens of GHz below the theoretical limit of f_{max}.

In addition to the limitations of f_{max}, the losses of the LC tank are also increasing with frequency. The low tank quality can be explained when combining Equation 4.6 and the respective expressions for the quality factor of an inductor and capacitor:

$$\frac{1}{Q_{tank}} = \frac{R_{Ind}}{\omega L} + \frac{\omega \cdot C_{Cap} \cdot R_C ap}{1} \tag{4.9}$$

For high frequencies, the total tank quality is dominated by the quality factor of the capacitive part of the LC tank, which decreases with frequency. This results in a higher resistance of the tank, and thus requires a larger negative-gm generated by the cross-coupled transistors, further reducing the maximum frequency where the steady-state oscillation requirements can be realistically met. Utilizing a process technology with a sufficiently high f_{max} will enable the implementation of fundamental THz VCOs [Seo11], such as InP, GaAs or SiGe (f_{max} of 130nm SiGe = 500GHz). In CMOS, fundamental signal generators have been reported at 270GHz in 32nm CMOS [Lan13]. However, with the f_{max} of current state-of-the-art nanometer CMOS technologies not exceeding 400GHz, fundamental oscillation in the THz range is currently impossible and unlikely to be achieved in the near future.

4.2 THz signal generation above f_{max}

If fundamental oscillation in the THz spectrum is (currently) not possible in CMOS, does this mean that THz CMOS circuits cannot be created using current CMOS processes? In other words: how can CMOS circuits operate beyond their f_{max} limits? The answer can be found when examining the f_{max} definition (Equation 2.5), which states that f_{max} is the highest frequency where power gain is achievable. While this puts a clear limit on amplifiers and fundamental oscillators, the f_{max} limit does not mean that there is no power present beyond f_{max}. In this work, this beyond-f_{max} power comes in the form of harmonics of below-f_{max} signals.

4.2.1 Harmonics above fmax

In most RF VCO and amplifier designs, harmonics are an unwanted effect due to the non-linear behavior of the components. Figure 4.5 shows a possible output spectrum of an amplifier with an ideal single-frequency input ω_0. The output of the amplifier will have a linearly amplified signal at the target frequency ω_0, as well as higher-order harmonics due to non-linear effects in the amplifier. These spurs caused by harmonic distortion are usually unwanted and suppressed or filtered, but can be beneficially used to generate power at a frequency multiple times higher than the (fundamental) input frequency.

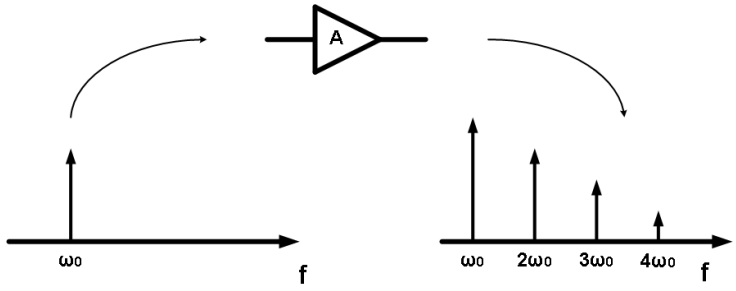


Figure 4.5: Harmonic distortion in an amplifier with a single-frequency input

Harmonics and the harmonic distortion of an input signal when going through a non-linear device is commonly represented using a power series representation. The relationship between input $x(t)$ and output $y(t)$ of the non-linear system can be represented by a power series:

$$y(t) = \alpha_1 \cdot (x(t)) + \alpha_2 \cdot (x(t))^2 + \alpha_3 \cdot (x(t))^3 + ... \tag{4.10}$$

In this equation, the α_n represent the non-linearity coefficients of the system, with exception of α_1 being the coefficient describing the linearized behavior of the circuit or small-signal gain of the amplifier.

For a single-tone input signal $Acos(\omega_0 t + \theta)$ with amplitude A, frequency ω and phase θ, Equation 4.10 becomes (limited to third-order components):

$$y(t) = \alpha_1 Acos(\omega_0 t + \theta) + \alpha_2 (Acos(\omega_0 t + \theta))^2 + \alpha_3 (Acos(\omega_0 t + \theta))^3 \tag{4.11}$$

$$\begin{aligned} y(t) = \alpha_1 A cos(\omega t + \theta) + \alpha_2 A^2 (\frac{1}{2} + \frac{1}{2} cos(2\omega_0 t + 2\theta)) \\ + \alpha_3 A^3 (\frac{3}{4} cos(\omega_0 t + \theta) + \frac{1}{4} cos(3\omega_0 t + 3\theta)) \end{aligned} \tag{4.12}$$

$$\begin{aligned} = \frac{\alpha_2 A^2}{2} + \big(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\big) cos(\omega_0 t + \theta) \\ + \frac{\alpha_2 A^2}{2} cos(2\omega_0 t + 2\theta) + \frac{\alpha_3 A^3}{4} cos(3\omega_0 t + 3\theta) \end{aligned} \tag{4.13}$$

Several observations can be made when examining Equation 4.13 [Wam98]. First of all, the second-order coefficient α_2 gives rise to both a DC component (DC offset) and a second harmonic component. If the fourth-order behavior was also included, this would give rise to an additional DC component and fourth harmonic presence. These even-order harmonics with α_i ; $i =$ even coefficients can strongly be reduced when using a fully differential circuit. The second observation is the nth harmonic amplitude will grow with the nth power of the input signal amplitude (A^n). An increase in input amplitude with 6dB will therefore increase the second harmonic amplitude with 12dB and the third harmonic with 18dB. This nth power relationship does not hold for large input amplitudes, as the power series representation of Equation 4.13 is valid for a small-signal system. A third observation is that the third-order non-linear coefficient α_3 also results in a fundamental frequency component which grows with A^3. Depending on the sign of this third-order contribution, this term would allow the fundamental frequency component to increase faster (gain expansion) or slower (gain compression) than linear. A final observation concerns the phase θ of the input signal: for an nth harmonic component, the phase is also multiplied with n. This means that any variation in phase at the fundamental frequency will be multiplied for the harmonics with the corresponding harmonic number.

The previous analysis assumed that there is no delay between the input and output of the system, and that the (non-)linearity coefficients are independent of frequency. This is called a memory-less or static non-linear system, and ignores the influence from capacitors and inductors in the system on the non-linear behavior. A more accurate way of modeling non-linear systems including these memory effects is the usage of Volterra series for distortion analysis [Bus74], where the coefficients describing the non-linear system behavior are frequency-dependent.

$$y(t) = H_1[x(t)] + H_2[x(t)] + H_3[x(t)] + ... + H_n[x(t)] + ... \tag{4.14}$$

In Equation 4.14, H_n is the nth order Volterra operator describing the nth order non-linearity of the system, with the nth order non-linear output of the system designated by $H_n[x(t)]$. The number of Volterra operators used to model the system can be increased depending on the input signal, which can accommodate the rising high-order harmonics with increasing input amplitude. A brief explanation of the setup of a Volterra series equivalent of a non-linear system is given in Appendix C.1. A more in-depth investigation into the calculation of the higher-order Volterra operators is beyond the scope of this work, but more information on this topic can be found in [Wam98].

4.2.2 Harmonic multipliers

From Equation 4.13 we found that by using harmonics, we can generate signals at multiples of the input frequency. The usage of these frequency multipliers (Figure 4.6) would allow us to generate power above f_{max}. A below-f_{max} signal ω_0 is used as an input for the multiplier system, and generates an output spectrum consisting of ω_0 and its harmonics, of which some (or all) can be present above f_{max}. Since these harmonics originate from the harmonic distortion of the multiplier and not from the amplification of an input signal at these frequencies, the f_{max} constraint is not violated. The unwanted harmonics, including the fundamental, can be filtered or suppressed by the circuit blocks that follow the harmonic generator.

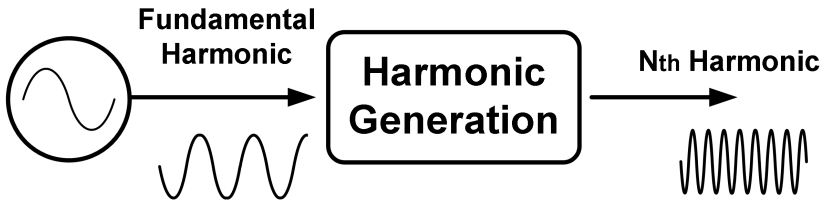


Figure 4.6: System overview of a N-factor frequency multiplier

Integrated harmonic multiplier circuits operating in the THz spectrum have been reported, including a stand-alone passive frequency doubler at 480GHz in 65nm CMOS [Han13a] and an active 325GHz frequency amplifier/multiplier chain (AMC) in SiGe [Oje11]. Amplifier/multiplier chains start from a low-frequency signal, which acts as the input for an amplifier driving a doubler/tripler/multiplier. This upconverted output is then further used as the input for a cascade of amplifier/multiplier combinations until the output reaches the target frequency. High-end measurement equipment used to generate signals in the mm-wave and THz bands are also based on amplifier/multiplier chains, with micro-machined Schottky diodes used as doubler/tripler blocks.

From the description of the multiplier operational principle, we can already define one of the issues of using harmonics as the wanted signal: the harmonic power is small in relation to the fundamental component. The resulting DC-to-THz efficiency will therefore be low, as the vast majority of the DC power is being consumed by the unwanted fundamental frequency component and (to a lesser degree) the other high-order harmonics. More importantly than the low DC-to-THz efficiency, this also implies that generating a high amount of output power above f_{max} through harmonics is a challenging endeavor. Power combining techniques can be used to increase the output power of a harmonics-based system by connecting the different harmonic generation cells together, paid for with an increase in absolute power consumption, chip area and system complexity.

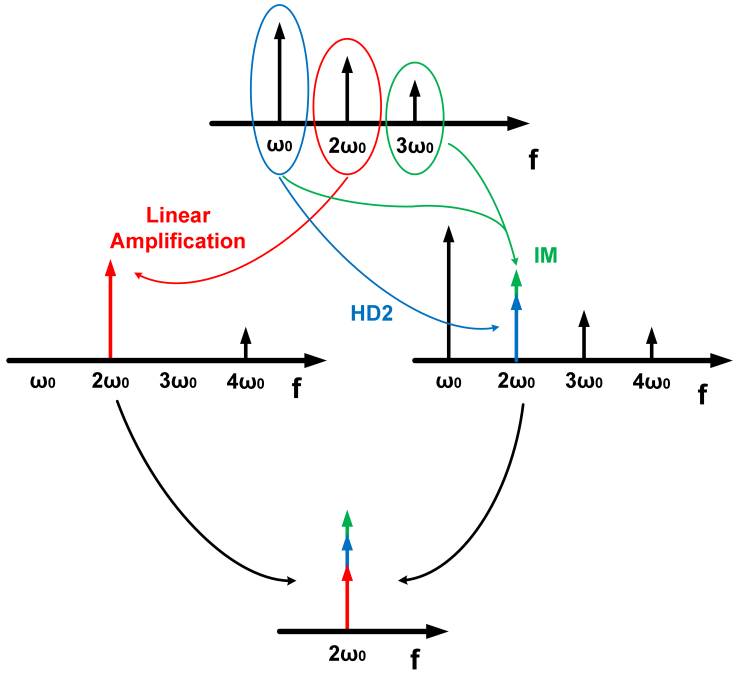


Figure 4.7: Second-harmonic generation through several mechanisms (linear amplification, harmonic distortion and intermodulation) and the combined result

Another way to increase the output power is to combine different harmonic signal generation mechanisms that contribute to the wanted harmonic, as depicted in Figure 4.7. In this example, the wanted frequency is the second harmonic of ω_0. Instead of an ideal single-frequency input, a signal with frequency ω_0 and its harmonics is applied to an amplifier. In addition to the second harmonic distortion (HD_2) of ω_0, the second harmonic $2\omega_0$ component at the input will be amplified (if there is any

gain at this frequency) and contribute to the total output power at $2\omega_0$. Further second harmonic contributions can originate in the intermodulation (IM) of the fundamental harmonic ω_0 and the third harmonic $3\omega_0$. The power generated at the nth harmonic can be drastically improved by these non-HD_N effects [Shi14], providing that there is sufficient gain (for the linear nth harmonic amplification) and harmonics power (for the IM contributions). Unfortunately, this is not the case for the THz frequency range of this work, but could prove to be very useful when designing circuits operating just below the f_{max} limit.

4.2.3 Harmonic oscillators

While harmonic multipliers use a VCO to generate the fundamental frequency to drive the multiplier, it is also possible to extract the harmonics of the VCO itself. While an ideal VCO would only generate the fundamental frequency, the non-linear behavior of the VCO transistor and components will also give rise to harmonics. When using a high-frequency VCO, its harmonics can reach into the THz range and therefore be used as an above-f_{max} signal generator. We will call these harmonic oscillators.

Similar to harmonic multipliers, the wanted harmonics are originating with the fundamental frequency of the VCO which will have a much larger output power than any higher-order harmonics present at the output of the oscillator core. Besides a lower DC-to-THz efficiency, this also means that the output signal will have a large unwanted fundamental component. However, by combining the multi-frequency component output signals of n oscillator blocks together, we can constructively combine the wanted nth harmonic component while canceling the other unwanted harmonics. Signal generators based on this concept are referred to as n-push oscillators [Yen03].

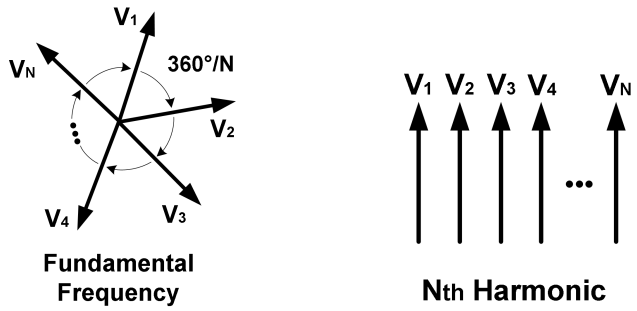


Figure 4.8: Phasor representation of the generated signals in an N-push oscillator at fundamental frequency (a) and Nth harmonic (b), which delivers the wanted signal

To illustrate the n-push oscillator concept, the phasor representation of n output signals at the fundamental frequency (summed together at one point) is shown in Figure 4.8a. If the phase difference between each adjacent fundamental phasor is kept at $360°/n$, the combined phasors will cancel each other and the sum of the fundamental frequency signals will be zero. However, as seen in Equation 4.13, the phase of the nth harmonic is also multiplied with n. As a result, the phasors of the nth harmonics will have a $360° = 0°$ phase difference with their adjacent phasor, illustrated in Figure 4.8. The phasors of the nth harmonic signals are all in-phase and will add constructively, resulting in a n-times larger signal at the nth harmonic. The zero-sum cancellation also applies to the other unwanted harmonics, which is demonstrated in Table C.2 and Figure C.2 for a n=4-push circuit.

A system view of an n-push circuit is given in Figure 4.9: the output signals V_i are generated in their respective cores, which are connected in such a way that the $360°/n$ phase difference requirement at the fundamental frequency is kept between neighboring cores. The signal cancellation for the unwanted harmonics and the constructive summation of the target nth harmonic is done in the n-way power combiner, which results in a nth harmonic output signal.

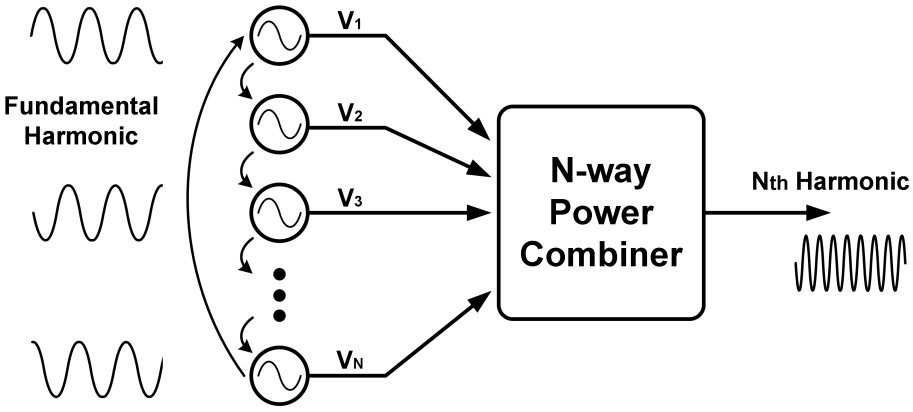


Figure 4.9: System overview of the underlying concept of an N-push oscillator

The usage of the n-push topology is very popular for generating high-frequency signals, and has been successfully used in CMOS to achieve above-f_{max} signal generation. Examples of these are a push-push (n=2) oscillator doubling a 205GHz signal to achieve a 410GHz signal in 45nm CMOS [Seo10a], a triple-push (n=3) oscillator at 480GHz in 65nm CMOS [Mom11] and a quadrature-push (n=4) oscillator at 553Ghz in 40nm CMOS [Shi11] consisting of two push-push VCOs coupled 180° out of phase.

The push-push implementation is usually a VCO where the second harmonic is extracted at nodes that are virtual grounds for the fundamental signal. In a cross-coupled oscillator, this is the center tap of the inductor, which is positioned on a virtual axis of symmetry between both sides of the oscillator. At this point, the signals from both sides of the oscillator are added together: the differential (180° phase difference) fundamental frequency component is canceled (AC ground) and the common-mode second harmonic is combined. The second harmonic can be extracted at this node with strongly reduced unwanted lower-order harmonic components.

4.3 0.54THz transmitter in 40nm CMOS

In recent years, the previously mentioned design methods have been used to implement integrated circuits at the high end of the mm-wave spectrum. By combining multiple oscillator cores together, transmitter output powers near and over 0dBm [Tou12] [Han13c] have been demonstrated. The fundamental frequency of VCOs and amplifiers have also increased with advancements in technology and modeling accuracy [Mom13] [Lan13] [Wan14] [Mog15], but these performance feats have yet to be achieved in sub-mm wave CMOS transmitters. The main reasons for this can be briefly summarized as follows:

- The absence of transistor gain, which results in the usage of low output power harmonics.
- Limited accuracy of transistor simulation models at mm-wave and higher frequency, as the measurement-fitted RF models are extrapolated beyond 30GHz.
- The limitations of circuit design options due to the low supply voltage and process layout requirements (Section 2.3.3).
- Increasingly dominant impact of the transistor's parasitic components (Section 2.2.2).
- The expanding modeling complexity of passives and interconnect structures at (sub)-mm wave frequencies (Section 2.3).
- Presence of the lossy silicon substrate and the need for on-chip antennas (Section 3.3) to get the THz signals on and off the silicon die.

In this section, we will present the design and measurements of a 0.54THz signal generator with large tuning range, fabricated in a 40nm bulk CMOS technology. An LC-VCO operating at 180GHz is connected to a non-linear buffer, designed to generate the wanted third harmonic at 540GHz. The wanted third harmonic is coupled through a

transformer to the output. The developed techniques are implemented on two different chips: a first version with a probe pad for on-wafer measurements [Ste13] and a second version with an on-chip planar dipole antenna, which enables us to use the transmitter in a THz imaging setup [Ste14]. Excerpts of these publications are reused in this section.

4.3.1 Third harmonic generation and extraction, from VCO to load

The objective of this work was to design a signal generator operating above 500GHz using harmonics. The circuit topology is shown in Figure 4.10. The THz signal generation starts with a LC-VCO with cross-coupled transistors to generate the fundamental frequency at 180GHz. The VCO is connected to a differential amplifier, which generates the third harmonic while also acting as a buffer between the output and the VCO core. This third harmonic is then coupled through a transformer to the output probe pad or dipole antenna.

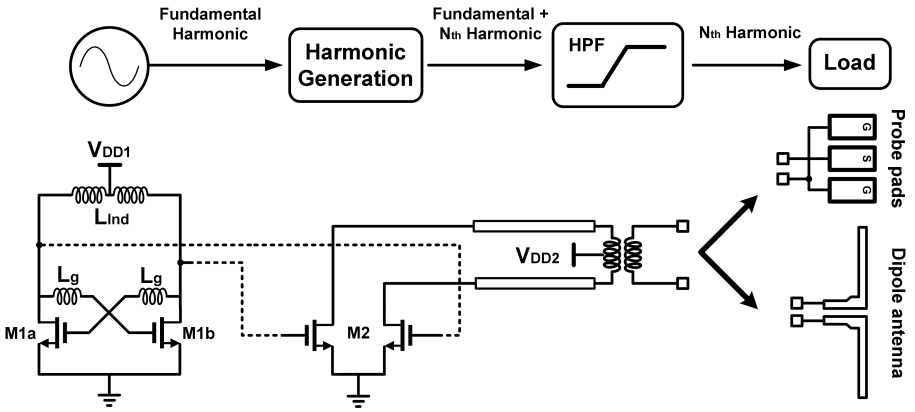


Figure 4.10: Schematic overview of the 0.54THz signal generator

VCO core and cross-coupled pair

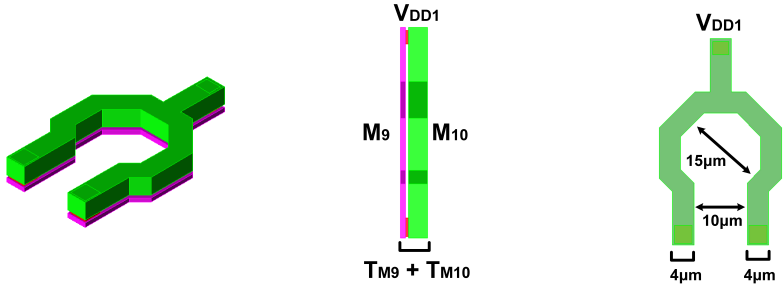
The starting point is choosing the fundamental frequency f_0 (below f_{max}) from which the harmonics (above f_{max}) will be derived. A low fundamental frequency is easier to generate but requires a higher order harmonic to reach the THz spectrum, which quickly degrades the output power. On the other hand, a high fundamental frequency

makes generating THz signals possible with a lower harmonics, but increases the design difficulty of the VCO as the fundamental oscillation nears the f_{max}. This work chooses the latter approach and uses the third harmonic of a 180GHz VCO. The fundamental oscillator is a LC-VCO with cross-coupled transistors to generate the negative resistance to compensate the tank losses (Section 4.1.3). As the oscillation frequency f_0 of the VCO is determined by the L and C components of the tank (Equation 4.15), these components become very small for near-f_{max} fundamental oscillation.

$$f_0 = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{tank} \cdot C_{tank}}} \tag{4.15}$$

$$= \frac{1}{2 \cdot \pi \cdot \sqrt{(L_{Ind} + L_{par}) \cdot (C_{CC} + C_{buffer} + C_{IMOS} + C_{par})}} \tag{4.16}$$

L_{Ind} is provided by a small, single-turn symmetrical inductor with a center tap for the VCO supply voltage, VDD1 (Figure 4.11). This inductor L_{Ind} determines not only the inductance of the LC-tank (and thus the fundamental oscillation frequency), but also the resistive losses that the cross-coupled transistors have to compensate. By using the top two metal layers in parallel instead of only one metal layer, the series resistance of the inductor is reduced, as well as a small reduction in inductance and SRF. The inductor has an inner diameter of 15µm and width of 4µm , resulting in an inductance L_{Ind} of 24.3pH and a Q-factor of 22.9 at 180GHz. The remaining inductance L_{par} comes from the parasitic inductance from the interconnection network.



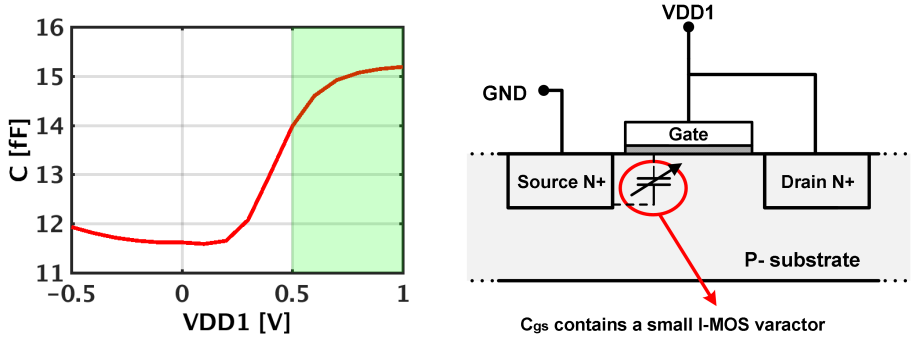
(a) (b) (c)

Figure 4.11: 3D representation of the single-turn VCO inductor which consists of the two top metals in parallel

Since the dimensions and values of L_{Ind} are so small, we should also consider the effects of process variations of the upper metals. The UTM can change both in thickness as well as in width. Tables C.3 and C.3 show respectively the inductance and quality

factor at 200GHz of an UTM inductor over the process corners for the thickness T and width W of the UTM trace. These are the worst case deviations of the nominal trace thickness and width, and we can see that the impact of process variation of the top metal itself is not too large.

In the majority of RF/mm-wave LC-VCOs, a varactor or switchable capacitor bank is placed in parallel with the tank inductor (Figure 4.3), between the drains of the cross-coupled transistors M1a and M1b. This variable capacitance allows tuning of the oscillation frequency by varying the capacitive part of the resonance tank [And00]. To effectively control the oscillation frequency, this varactor should be sufficiently large compared to the other (parasitic) capacitances. However, a large tuneable capacitor would add additional capacitance to the tank and lower the LC product, decreasing the oscillation frequency of the oscillator which we want to be as high as possible. In addition, the quality factor of capacitors decreases with frequency (Equation 2.17), which would reduce the overall quality of the LC tank (Equation 4.6). For these reasons, the tuning capacitor was omitted from the LC tank. The resulting tank capacitance comprises of the capacitances of the cross-coupled pair M1 (C_{cc}), buffer transistors M2 (C_{buff}) and the parasitic capacitance of the inductor and interconnect (C_{par}). Even though no tuning element was added to keep the tank components small, the frequency can still be controlled: the gate-source capacitance C_{gs} of the cross-coupled transistors, which contains a parasitic inversion-MOS varactor C_{IMOS}, can be varied by changing the biasing voltage (=supply voltage VDD1), as shown in Figure 4.12.



(a) (b)

Figure 4.12: Capacitance variation (a) and location (b) of the parasitic I-MOS varactors in one of the cross-coupled transistors

This variation in capacitance of one transistor is only a few femto-Farads and can usually be neglected compared to the fixed tank capacitance or tuning capacitor in RF VCOs. However, in this design, no tuning capacitor is added and the fixed capacitance is kept small to achieve an oscillation frequency as high as possible. Therefore, impact

of this parasitic I-MOS varactor on the tank capacitance becomes large enough to allow 'parasitic tuning' of the LC tank (and thus resonance frequency) by modifying the supply voltage of the VCO core (Figure 4.13).

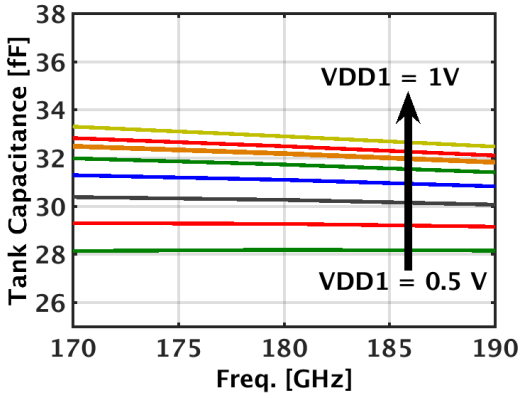
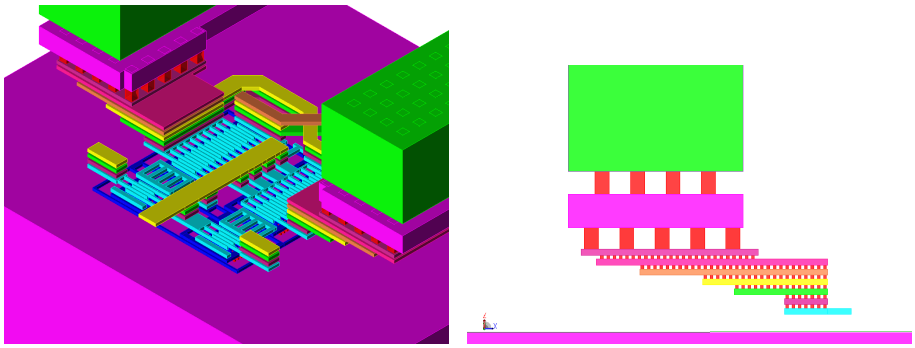


Figure 4.13: By changing the supply voltage VDD1, the capacitance of the cross-coupled transistor pair can be varied and used as a tuning element

Besides capacitance for the tank, the cross-coupled pair also provides a negative resistance to compensate the resistive losses in the LC tank. Parasitic effects that are otherwise non-dominant can have a critical impact when designing sub-mm wave circuits. It is therefore important that the transistor models include this high-frequency behavior. While the f_{max} of a small, minimal dimensions transistor is above 300GHz in 40nm CMOS, the practical limit on a transistor's speed will be lower due to the transistor size, layout and wiring.

To maximize the f_{max} of M1 and M2, all transistors have double-contact gates to reduce the gate resistance R_g and narrow, 1µm fingers. C_g and C_d of transistors M1 form the majority of the capacitive part of the LC-tank. To reduce C_g, metals 3-6 were used in parallel for the cross-coupling connection of the M1 transistors, as lower metal layers would result in a larger C_{gb}. The parallel metal traces reduce the series resistance of the connection. The layout of the VCO core is shown in Figure 4.14a.

One important detail is the connection between the drain of the M1 transistors in the bottom metal layer and the leads of the inductor, in the top 2 metal layers. The capacitance and more importantly the series resistance of this via stack connection is added to the losses of the tank. Using a small via stack straight to the top metals would keep C_{db} small, but would introduce a larger series resistance. Especially in deep-scaled nanometer CMOS technologies, where the metal via resistance increases with technology node, this is an important aspect to be considered. As this series resistance would add to the resistive losses of the tank, a larger negative resistance



(a) (b)

Figure 4.14: 3D view of the VCO core layout (a) and sideview of the tapered viastack connection between the transistor and inductor lead (b)

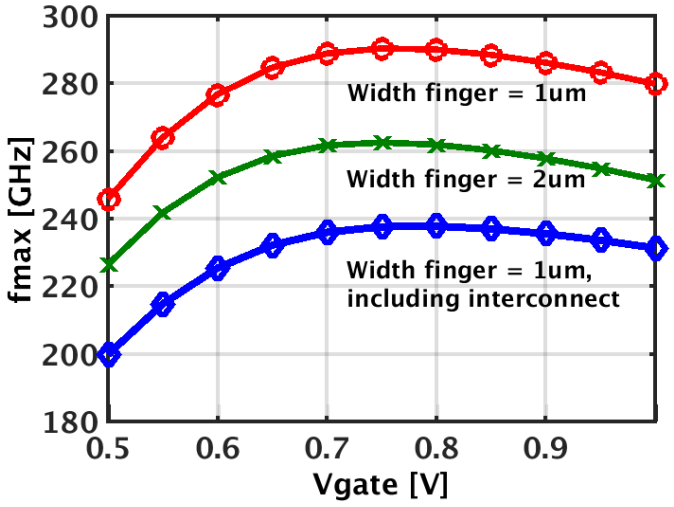


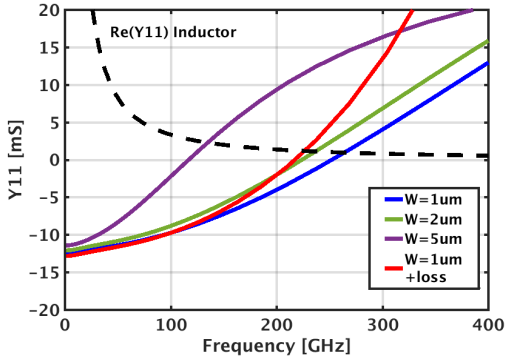
Figure 4.15: Simulated f_{max} of transistors with the same W/L ratio (20µm/0.04µm) but different width and number of fingers configuration. The graph shows the difference in f_{max} for two stand-alone RF transistors, and one including the interconnection network

has to be generated to allow the oscillator to start up. A big via stack, on the other hand, would have a lower series resistance due to the larger number of parallel metal vias, but a larger overlap of lower-layer metal and substrate, creating a larger C_{db} and reduce the oscillation frequency of the VCO. To optimize this interconnect, the via stack was given a tapered shape (Figure 4.14b): narrower at the bottom, to minimize the metal-substrate overlap capacitance, and getting wider to allow for more vias at higher metal layers, where the substrate coupling capacitance is less. To illustrate the influence of both transistor and interconnect layout on f_{max}, Figure 4.15 shows the simulated f_{max} for two RF model transistors without the interconnect network (similar to the discussion from Section 2.2.2), and the same transistor with the interconnection metals. The f_{max} limit drops about 50GHz to 240GHz.

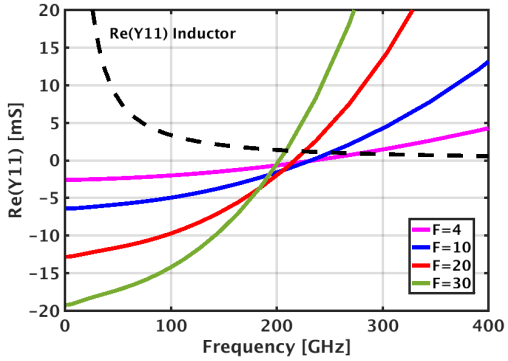
While f_{max} is a useful metric to determine the high-frequency potential of a design, ultimately the purpose of the cross-coupled pair is to generate a negative resistance. Figure 4.16a shows the real part of $Y_{cross-coupled}$ for different cross-coupled transistor finger widths ($F = 20$). The frequency where the negative resistance crosses from negative to positive is f_{gm}. Similar to the impact on f_{max}, the optimal transistor finger width yields a larger negative resistance up to a higher f_{gm}. Utilizing the same $W = 1\mu$m finger width we found to be optimal for the f_{max} of a single transistor, we find that the f_{gm} of the cross-coupled pair is 253.4GHz compared to 117GHz for a transistor pair with $W = 5\mu$m. Addition of the metal traces creating the cross-coupled connection between the transistor gates and drains, as well as the tapered via stack to the inductor leads, reduces the f_{gm} to 218.3GHz. The plotted $Y_{cross-coupled}$ in Figure 4.16 may seem too small at 180GHz to compensate the tank losses, but this value already accounts for the losses of the transistors' parasitic capacitance. As we mentioned earlier, the LC tank of the VCO consists of the inductance of the inductor and the parasitic capacitance of the VCO core transistors. The tank losses are the combined parallel losses of the inductor and capacitor, of which the low quality factor of the parasitic capacitances will dominate at 180GHz (Equation 4.6, where the quality factor of inductors increases with frequency). As these parasitic capacitances and their tank-dominating losses are included in the cross-coupled transistor simulation, the resulting $Y_{cross-coupled}$ should be large enough to compensate the remaining loss of the inductor (Y_{Ind}), also shown in Figure 4.16.

As the generated negative resistance diminishes with increasing frequency (Equation 4.8), the size of the M1 transistors has to be increased to adequately compensate the inductor/tank losses (Figure 4.16b). Smaller cross-coupling transistors generate a lower negative resistance, but remain negative up to a higher f_{gm} than large M1 transistors (235.9GHz for $F = 4$ versus 203.6GHz for $F = 30$). Unfortunately, larger transistors also increase parasitic capacitance (9.2fF for $F = 4$ versus 45.5fF for $F = 30$), lowering the LC tank's resonance frequency.

To alleviate this trade-off, an inductor L_g can be placed between the gate and drain of the cross-coupling connection. The presence of these inductors will increase the



(a)



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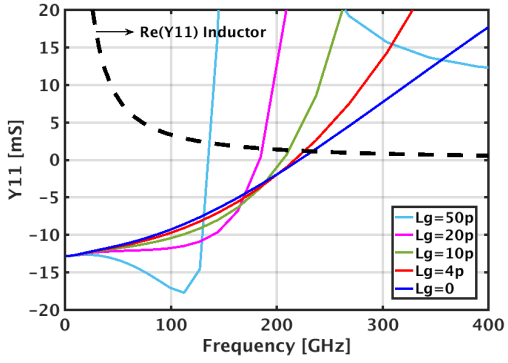


(c)

Figure 4.16: Generated negative resistance by a cross-coupled pair for different (a)finger width W ($F = 20$), (b) number of fingers F ($W = 1\mu$m) and (c) gate inductance L_g ($W = 1\mu$m, $F = 20$)

parasitic capacitance of the cross-coupled pair, but fortunately also increases the performance of the transistors to generate a larger negative resistance [Li09]. In turn, for identical tank losses, this means that smaller transistors can be used to generate the same required negative resistance at the target frequency, resulting in a smaller total tank capacitance. In this design, the connection between the drain and gate of the cross-coupled transistors are small metal traces that form small series inductors which can be used for this negative resistance boosting technique. Figure 4.16c shows the resulting $Y_{cross-coupled}$ for increasing values of L_g. While using large gate inductors definitely shows a peak in performance around 100GHz [Vol11], the decline of the negative resistance beyond this peak is steep, resulting in f_{gm} that do not reach the target frequency of 180GHz (138.9GHz for $L_g = 50$pH versus 218.3GHz for $L_g = 4$pH). While designing the cross-coupling connection, we should make sure that the parasitic L_g inductance is large enough to improve the negative resistance generation without becoming too large and peak too early, with a f_{gm} below the target frequency.

Harmonic generation and transformer network

Transistors M2 create the non-linear buffer that isolates the LC-tank from the load and generates the wanted third harmonic. The transistor size is kept small, as the gate capacitance of the buffer will further load the LC-tank and reduce the oscillation frequency. The buffer/non-linear amplifier is driven by the 180GHz signal of the VCO,and generates the third harmonic at 540GHz.

$$I_{out,3\omega} = Y_{21,3\omega}V_{in,3\omega} + Y_{22,3\omega}V_{out,3\omega} + \alpha_1 V_{in,\omega}^3 + \alpha_2 V_{out,\omega}^3 \tag{4.17}$$

From Equation 4.17, the output third harmonic will firstly depend on the linear amplification of the third harmonic components at the input and output. Secondly, the non-linear components generated by the distortion of input and output fundamental components could also contribute. Since the third harmonic of 540GHz is well above the f_{max} of the transistors, the third harmonic input signal (3ω generated in the VCO) will be strongly attenuated. The output third harmonic will thus completely depend on the non-linear distortion of the fundamental frequency of the VCO at 180GHz.

To improve the generation of the third harmonic, the voltage swing of the VCO signal which is applied at the gates of the buffer, should be large: from Equation 4.13 and Equation 4.17, we found that increasing the fundamental amplitude will increase the third harmonic with a third power. To maximize the VCO swing, the traditional current-biasing transistor between M1 and VDD1 is removed to increase the voltage headroom. Additionally, the supply voltage of the buffer (VDD2) is chosen differently from the VCO core to improve non-linear operation. The gate bias of the non-linear buffer is VDD1, the supply of the VCO core. Simulations showed that a VDD2 of 600mV

resulted in the highest amount of output power at the third harmonic (Figure 4.17). Due to the differential nature of the VCO and harmonic generating buffer, there is almost no second or fourth harmonic signal present.

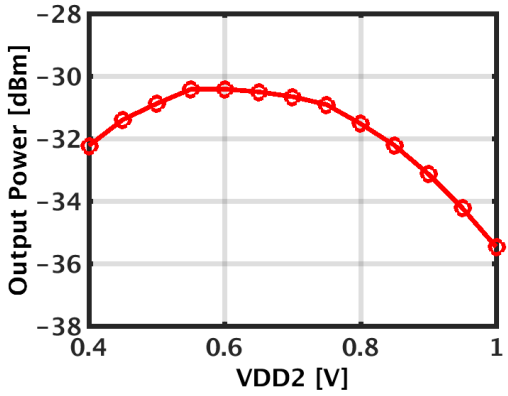
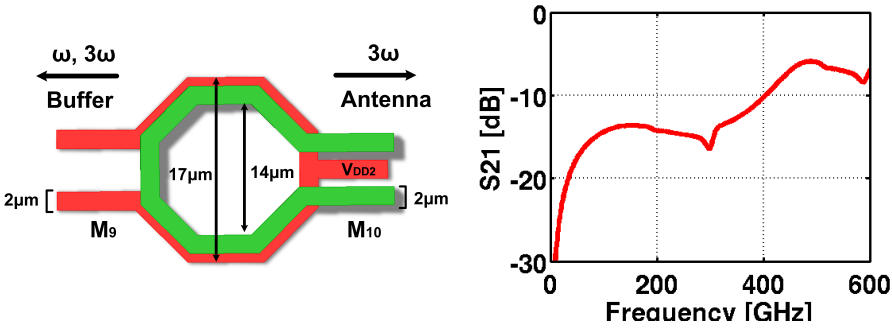


Figure 4.17: Output voltage waveform (a) and third harmonic output power (b) for varying VDD2

After generation, the third harmonic is coupled to the output using a transformer. The buffer transistors still have to operate at the fundamental frequency, as the third harmonic's power is related to the fundamental signal. There are two frequencies of interest for the TL/transformer network, the fundamental and the third harmonic. The transformer network should act as a high-pass filter for the third harmonic and attenuate the fundamental frequency. The secondary winding of the transformer is connected to the load and is matched with the probe pads/antenna at 540 GHz. Simulations show that the whole coupling structure, which starts at the drains of the M2 transistors and ends at the input of the load, favors the transfer of the third harmonic to the output over the fundamental frequency (Figure 4.18).

The transformer used in the buffer is implemented as two coupled single-turn inductors in the top two metal layers. To keep the self-resonance frequency (SRF) of the transformer windings above the third harmonic, small inductor diameters and narrow trace widths are used. This is to avoid the very sharp variations in impedance at the self-resonance of the transformer's windings. The primary (17µm) and secondary winding (14µm) have different diameters, as this is a trade-off between the higher SRF of a planar transformer and the better coupling of a stacked topology. The inductor on the buffer side includes a center tap for the biasing of the M2 transistors through differential transmission lines ($Z_0 = 130\Omega$).



(a) (b)

Figure 4.18: Simulated S_{21} for the coupling of fundamental and third harmonic from the buffer drain node to the output

4.3.2 Antenna and probe design at 0.54THz

Once the signal at 540GHz is generated, it has to be taken off-chip to be measured. From Chapter 3, the two most viable options for THz signals are using high-frequency probes for on-chip circuit verification and on-chip antennas for radiation measurements. Both methods have been applied to this design.

WR1.5 probe pads

While using probes is only useable in a laboratory environment, it provides one of the most accurate measurement methods to characterize the behavior of the fabricated circuit. The output signal falls in the WR1.5 frequency band, which ranges from 500GHz to 750GHz.

As mentioned in Section 3.2, the dimensions of probe pads reduces with increasing frequency due to the smaller pitch of the probe tips. The size of the probes also has an impact on the transmission of the THz signal. Large GSG pads provide a larger capacitive coupling to the substrate, and longer pads increase the fringe capacitance between the two ground pads and the signal path. Both effects are detrimental at sub-mm wave frequencies, and result in lower transmission of the signal towards the 50Ω load. Using probe pads that are too small, however, will prove to be more difficult to reliably land the probe tips. From this, we conclude that the probe pads should be kept to a minimum while still accommodating the manual landing of the probe tips. Each probe pad is 25µm wide and 40µm long (Figure 4.19). The pitch of the WR1.5 probe is 30µm, and should thus also be the pitch for the on-chip probe pads.

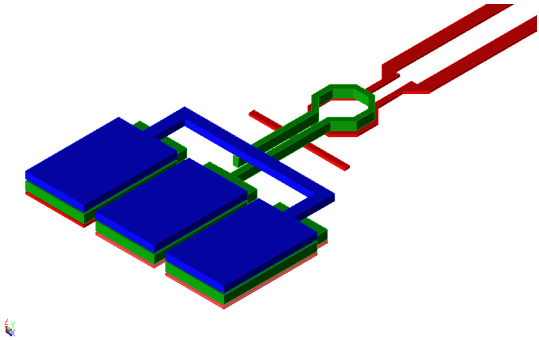


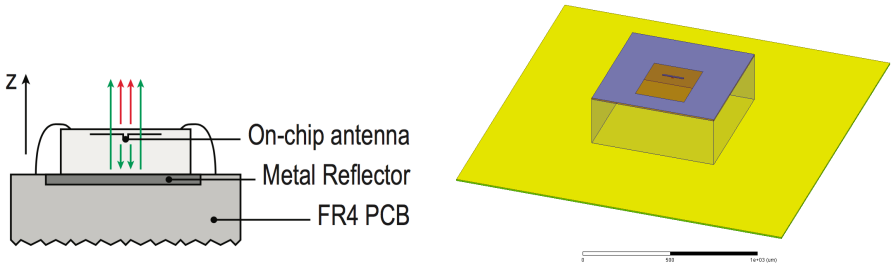
Figure 4.19: 3D model of the WR1.5 probe pads, connected to the transformer and differential transmission line

On-chip planar dipole antenna

To also be able to radiate the generated THz signal off-chip without probes, an on-chip antenna was designed and fabricated together with the signal generator. While a high-directivity on-chip patch antenna would increase the radiation performance of the transmitter, an antenna with a medium to large bandwidth was preferred to mitigate any process variation effects on the effective oscillation frequency. Also, since this is the first on-chip antenna designed at these frequencies by this research group, the decision was made to go for a dipole antenna.

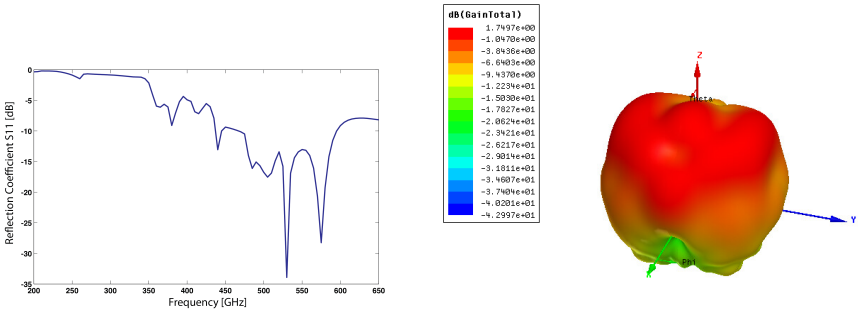
The chip would be placed on a FR-4 PCB to be wire-bonded for the DC connections, as flip-chip was not yet an option. As mentioned in Section 3.3.2, a large portion of the radiated signal is being directed into the substrate. To recover a part of this substrate radiation, a metal reflector plane is placed on the FR-4 board under the die. This large copper plane will reflect the backside radiation with a 180° phase shift. If the distance between the antenna and the reflector is chosen to be an odd multiple of a quarter wavelength, the reflected signal will constructively add to the front-side radiation and increase the radiated power towards the detector.

The simulation setup is shown in Figure 4.20, which includes the FR-4 PCB board, the silicon substrate and the surrounding metals around the antenna. The simulated reflection coefficient(Figure 4.21a) shows a low S11 over a broad frequency bandwidth around the desired third harmonic signal. Due to the differential nature of the signal source, the unwanted second and fourth harmonic signal are suppressed. Simulations using ANSYS HFSS show a peak gain of 1.75dBi (Figure 4.21b) and a radiation efficiency of 19% [Thi15].



(a) (b)

Figure 4.20: Simulation setup for the on-chip dipole antenna in HFSS, including FR-4 with copper reflector



(a) (b)

Figure 4.21: Reflection coefficient (a) and simulated radiation pattern (a) of the on-chip dipole with reflector

4.3.3 Measurement results

Using the above-mentioned techniques, two chips were implemented in 40nm CMOS and measured: one with a probe pad and one with an on-chip dipole antenna. Measuring sub-mm wave signals is a challenging endeavor, as the high losses of the measurement equipment at these frequencies make it hard to detect the THz output signals. Other works at these frequencies use a quasi-optic measurement approach [Seo10a] [Shi11] where an on-chip antenna radiates the signal into a Fourier-transform infrared spectroscopy (FTIR) system with sensitive, liquid nitrogen cooled bolometers to be able to detect the THz signals. Measurements in the presented work were done using a VDI MixAMC with sub-harmonic mixer for the 500-750GHz band. The output of the mixer is connected to a R&S FSU Spectrum Analyzer. The spectrum

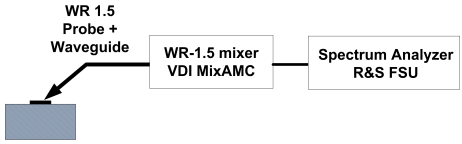


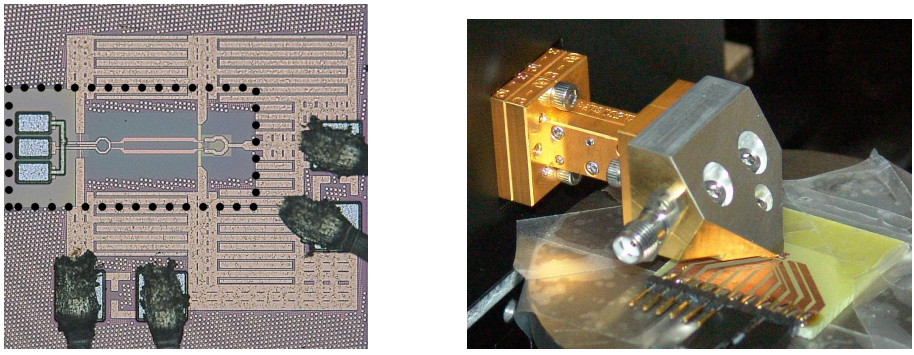
Figure 4.22: Schematic representation of the measurement setup when using WR1.5 probes

analyzer was calibrated using an Erickson PM4 power meter and a VDI AMC source module.

Probe

For the on-wafer measurements, this work uses a high-frequency probe and downconverter to accurately determine output frequency and power of the 540GHz signal generator. The measurement setup is shown in Figure 4.22. It consists of a WR-1.5 DMProbe [Wei11] attached to a VDI MixAMC WR1.5 downconverter.

Figure 4.23a shows the chip photo of the 0.54THz transmitter with WR1.5 probe pads. The active area is 110µm x 300µm and the total chip area including bond pads and decoupling is 350µm x 430µm. Figure 4.23b shows a close-up of the WR1.5 probe while landed on the chip.



(a) (b)

Figure 4.23: 0.54THz transmitter die photo (a) and probe closeup

The output spectrum of the signal generator when being probed is shown in Figure 4.24, showing a clear signal peak. The measurement results and comparison with simulations are displayed in Figure 4.25. Measurements show good agreement with simulation

results, indicating correct modeling of the passives and RF transistor's behavior at frequencies above fmax. When the supply voltage of the buffer, VDD2, is fixed at 650mV, the VCO starts oscillating at 561.5GHz for VDD1 = 540mV. By changing the supply voltage of the VCO core, a 21.9GHz tuning range is measured (539.6GHz to 561.5GHz). After accounting for the losses of the probe and mixer, the peak output power is -31dBm at 543GHz, with a DC power consumption of 16.8mW for a VDD1 of 800mV. If the tuning range is limited to frequencies with an output power within 3dB of the 31dBm peak, the tuning range becomes 5.5GHz, stretching from 539.6GHz to 545.1GHz. Thanks to the fully differential approach, even harmonics are suppressed in favor of the uneven harmonics: the fourth harmonic at 730GHz did not rise above the noise floor, meaning that its output power is at least 30dB lower than the wanted third harmonic. Fundamental and second harmonic could not be measured in the on-wafer version because of the small bond pad pitch required for the WR1.5 probe. The simulated phase noise at 543GHz is 69.6dBc/Hz at 1MHz offset.

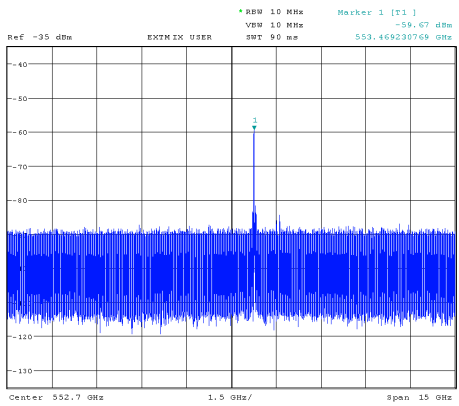
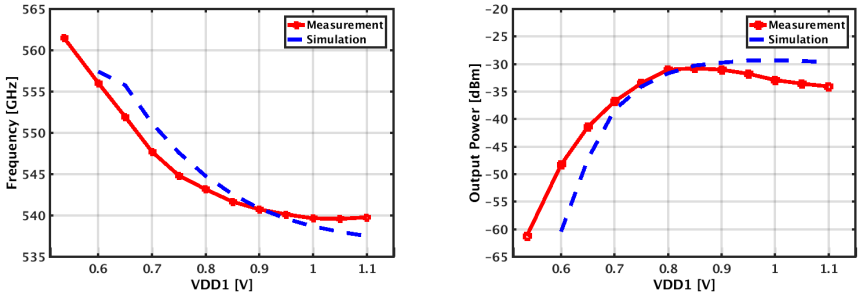


Figure 4.24: Output spectrum of the 40nm CMOS signal generator when measured with probe

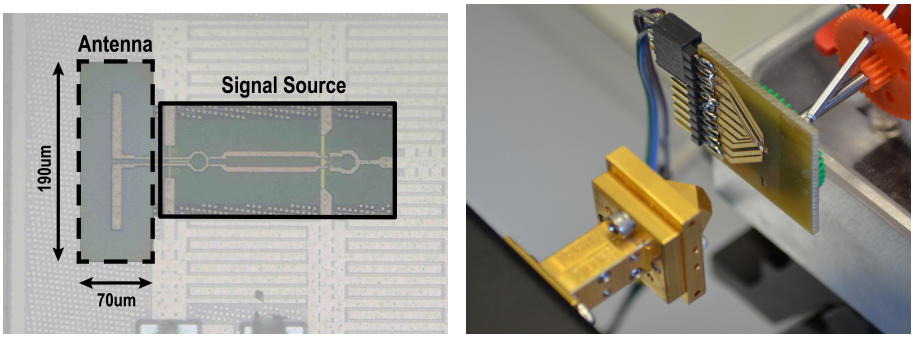
Radiation version

Besides a break-out version with only the signal generator and a probe output, a version with the on-chip dipole antenna is fabricated and measured (Figure 4.26). The active area is 170µm x 300µm and the total chip area including bond pads and decoupling is 350µm x 430µm. The radiated signal is picked up by a WR1.5 horn antenna (Figure 4.26b) connected to the VDI MixAMC. The down-converted IF signal is measured by a spectrum analyzer, which then shows the output frequency and strength of the signal. An example of the measured output spectrum is shown in Figure 4.27.



(a) (b)

Figure 4.25: Measurement results of the probe version, showing frequency variation and power fluctuation with varying VDD1



(a) (b)

Figure 4.26: Die photo of the transmitter with on-chip dipole antenna(a) and antenna close-up

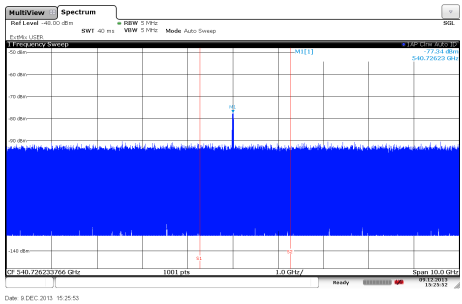


Figure 4.27: Output spectrum of the 0.54THz signal generator with on-chip antenna, before accounting for losses

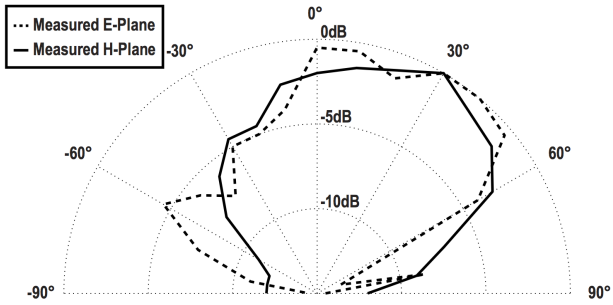


Figure 4.28: Normalized radiation pattern of the 0.54THz transmitter with on-chip dipole antenna

As mentioned in Section 4.3.2, the substrate radiation is a major loss contributor. To recuperate some of this substrate radiation and redirect it towards the top direction, a reflector was implemented on the FR-4 PCB. The distance between the transmitter and the receiving antenna was 20mm to fulfill the radiating far-field region criterion (Equation 3.10).

By rotating the radiating chip over its E and H-planes, the radiation pattern can be measured. The resulting radiation patterns are shown in Figure 4.28. Using Friis formula (Equation 3.9), the Equivalent Isotropically Radiated Power (EIRP) was calculated to be -31.8dBm for one chip. This EIRP can be improved by using antenna arrays or (substrate) lenses to increase the radiated power and directivity. These devices were not used in this work, as this would increase cost and packaging requirements of the transmitter. Assuming the simulated antenna gain of 1.75dB is correct, the estimated radiated power of the transmitter is -33.55dBm $(EIRP_{dB} - G_{antenna,dB})$. The radiated 180GHz fundamental signal was measured using a pyramidal horn antenna and a RPG

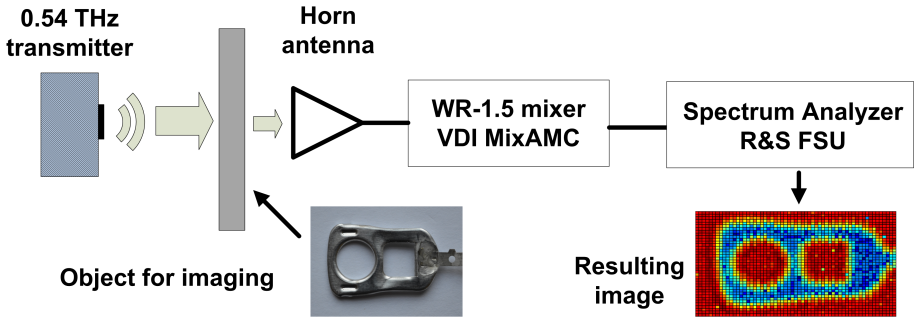


Figure 4.29: Measurement setup for a mechanically stepped 1-pixel 0.54THz imager. A metal soda can lid and its THz image are shown

WR-05 sub-harmonic mixer for the 140-220GHz band. The resulting fundamental EIRP is -22.8dBm. Additional matching/filter networks between the transformer and antenna could further reduce the transmission of the fundamental signal. The peak received radiated signal at 540GHz is 14dB above the receiver's noise floor, which is -45dBm in the wireless setup.

4.3.4 0.54THz imaging results for dielectric contrasting

To demonstrate the capabilities of lens-free THz CMOS imaging, the fabricated 0.54THz transmitter with on-chip antenna is used as a source in a THz imaging system. The antenna measurement setup used for the radiating transmitter characterization can be considered as a 1-pixel imaging setup, where the THz transmission at one small, specific point in space is being measured. If we place an object between the THz transmitter and the WR1.5 downconverter (receiver), the THz absorption of this object on this specific point is measured. By mechanically moving the object, the setup depicted in Figure 4.29 can scan the object for the THz transmission on a grid of points, thus resulting in a THz image of the object based on detection of the transmitted THz power.

The first object that was scanned is the metal lid of a soda can. The metal reflects the THz signal, and as a result no THz power is detected by the receiver when the metal lid is positioned between transmitter and receiver. Using a mechanical stepper moving the lid in the XZ plane withsteps of 0.5mm, the whole object is scanned. Both the visible and THz image of this soda can lid are shown in Figure 4.29.

While metal does not allow a radiated THz signal to be transmitted, different materials

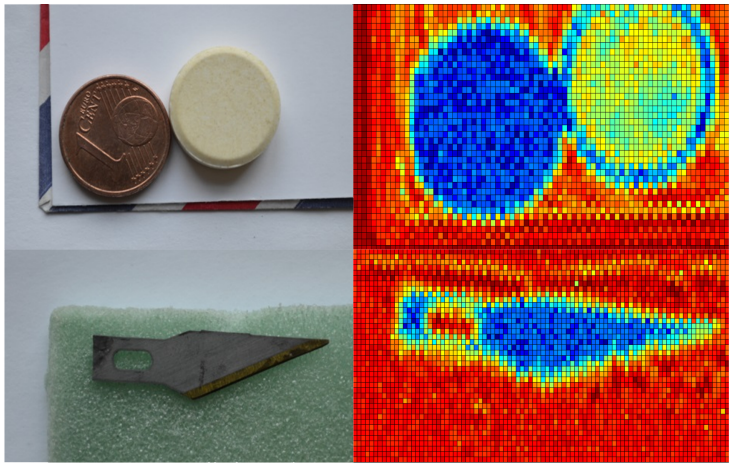


Figure 4.30: Dielectric contrast imaging results for a coin, name card and vitamin tablet inside an envelope (top) and scalpel head in foam (bottom). Red colors indicate full THz signal transmission, blue colors indicate no THz signal transmission due to reflection or absorption by the object

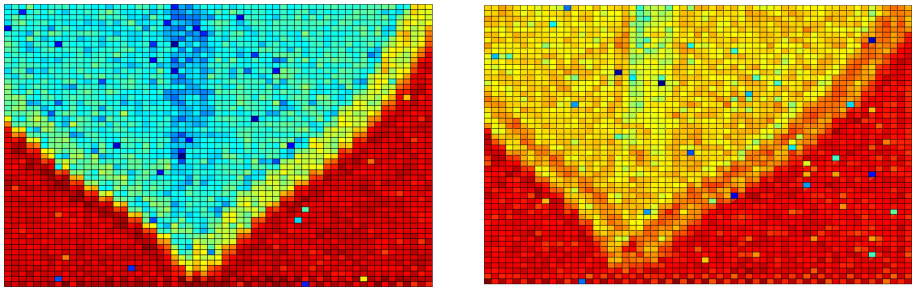


Figure 4.31: Measured difference in water concentration of a freshly cut (a) and dried for 48 hours (b) orange tree leaf. The remaining water content of the dried leaf is concentrated in the stem. Red colors indicate full THz signal transmission, blue colors indicate no THz signal transmission due to absorption by the water molecules in the leaf

show different THz behavior. These differences can be used for detecting metal pieces in materials that are transparent for THz radiation, such as the foam shown in Figure 4.30. A metal scalpel head was hidden in the foam, and can very clearly be seen in the THz image. A similar experiment with a metal coin and a vitamin tablet inside an envelope illustrates that the THz imaging setup can distinguish the material composition of two objects with the same form factor. Industrial production lines could use this type of dielectric contrast information for non-destructive quality control.

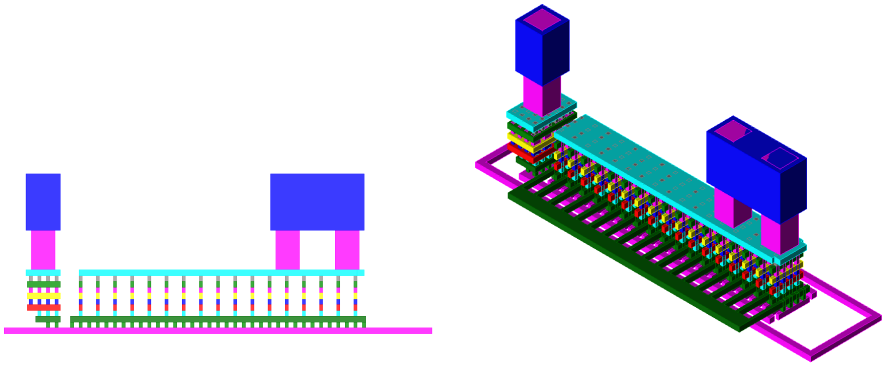
One of the more interesting aspects of the 0.54THz transmitter is the fact that there is a large absorption peak in the frequency spectrum located at this frequency for water: even small amounts of water will provide a very large attenuation of the signal. While this can pose a problem when trying to communicate over long distances in rainy or foggy conditions, this also allows us to make a water detector. This type of measurements can be used in an agriculture setting, where the plant stress due to drought can be monitored [Bre11]. Figure 4.31 illustrates this plant health monitoring by showing the THz image of an orange leaf when freshly cut and after drying the leaf for 48 hours, showing that the water contents have drastically reduced.

4.4 0.57THz and 0.6THz transmitter in 28nm CMOS

With the scaling of CMOS, the initial assumption is that a smaller technology (shorter gate length L) is always better. While the intrinsic speed of a smaller technology is indeed faster, the constraints and requirements to reach it are also becoming more and more difficult to meet. One could state that the intrinsic devices are getting faster, but connecting to the device is getting more difficult. During the design in 28nm, we will discuss how far the designs of the previous section can be pushed [Ste15]. To push the frequency limit, two fully integrated signal sources with on-chip antenna are implemented in 28nm bulk CMOS to generate above-fmax signals using harmonics. A VCO is driving a non-linear amplifier, which generates the wanted third harmonic. This signal is coupled to the on-chip antenna by two different approaches: directly to a folded dipole antenna or to a collinear dipole antenna through a transformer. The results are 570GHz and 600GHz signal sources, which are used as transmitters in a THz imaging setup for non-destructive testing. Thanks to their small silicon footprints, the sources would allow high-pixel density transmitter arrays for lens-free THz imaging [Ste16].

4.4.1 Vertical transistor layout for high mm-wave operation

When moving from 40nm to 28nm, several changes in design process are required. At the time of design, no RF models were available in the 28nm technology. Since this meant that the transistor interconnect layout could be designed from scratch, the design of the cross-coupled core was optimized. Ultra-low VT (ULVT) transistors with gate contacts on both sides were used to increase the maximum oscillation frequency of the cross-coupled pair. This provides the optimized trade-off between gate resistance and routing capacitance. To further reduce the parasitic capacitance, the transistor gate and drain metals are stacked up (Figure 4.32) and the routing to and from other transistors is made in metal layer 6, thus reducing the capacitance to the substrate [Zha13].



(a) (b)

Figure 4.32: Vertical transistor layout in 28nm CMOS to reduce the gate-drain overlap capacitance

Using this transistor layout, the f_{max} for both NMOS and PMOS is simulated and presented in Figure 4.33. The NMOS transistor is still faster than its PMOS counterpart, but the difference is not as large as in previous nodes, indicating the progress of PMOS performance relative to NMOS.

An important observation can be made when evaluating the optimal finger width of a transistor. The analysis for a 40nm CMOS process concluded that there is an optimal finger width of approx. 1µm, where a trade-off exists between decreasing R_g and increasing parasitic capacitance of the interconnection (Figure 2.12). In a 28nm CMOS process, this optimum is no longer valid: the impact of R_g remains the dominant component determining the f_{max} of the transistor, even for narrow finger width W. As the decrease in R_g keeps outperforming the increase in parasitic capacitance, the minimal finger width of 600nm should be utilized to achieve the highest f_{max}

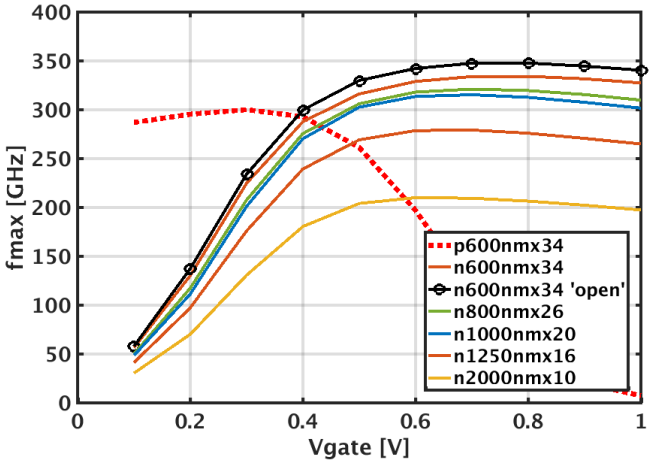


Figure 4.33: Simulated f_{max} for different transistor widths, including a PMOS transistor

(347.8GHz) possible. Appendix C.5 further highlights the impact of even small layout modifications of the double-gate connection to the f_{max}.

4.4.2 Design of VCO core for 28nm THz transmitter

The schematic of the transmitter with transformer and collinear dipole antenna is shown in Figure 4.34. The VCO generating the fundamental frequency around 200GHz is a cross-coupled LC VCO. As the transistor layout used in 28nm is a stacked layout up to metal 6, routing and connecting the core transistors to the inductor leads is done in this layer. In addition to the thicker metal (reduced series resistance), this also keeps the overlap capacitance low by staying away from the lossy silicon substrate.

The isometric (a) and side view (b) of the transmitter core layout are shown in Figure 4.35. By mirroring the core transistors, the gate-drain interconnection to create the cross-coupling of the two transistors becomes very compact. On each side of the VCO core, the drain, gate and inductor lead can be connected with a 1µm metal 6 trace. The layout also reduces the gate-drain line overlap and thus C_{gd}, which together with gate resistance form the dominant limiters on high-frequency performance. In addition, the gate inductance L_g is kept to a minimum. The tank inductance itself is kept small by using a single-turn inductor. On-chip inductors greatly benefit from the availability of an top ultra-thick metal to reduce the trace resistance. As this UTM was not part of the metallization scheme, L_{Ind} is implemented by combining the 3 highest metal layers

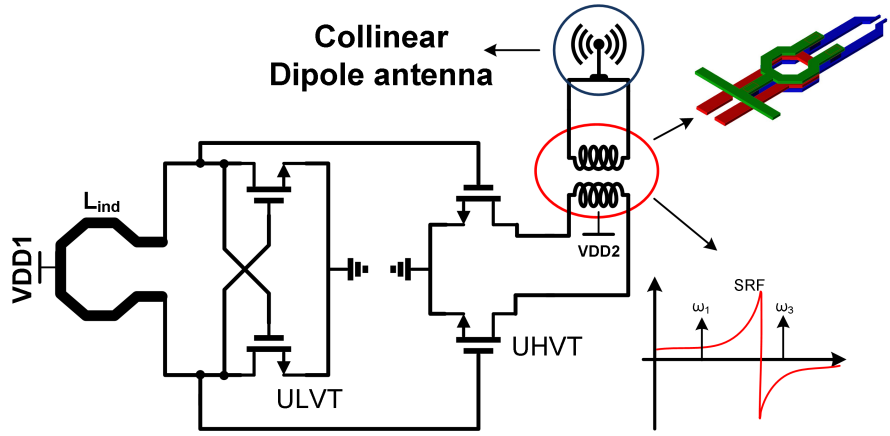
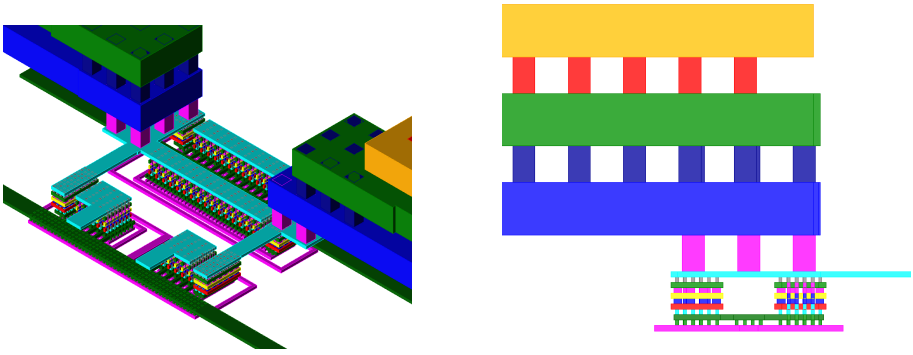


Figure 4.34: Schematic of the 28nm CMOS transmitter with transformer and on-chip collinear dipole



(a) (b)

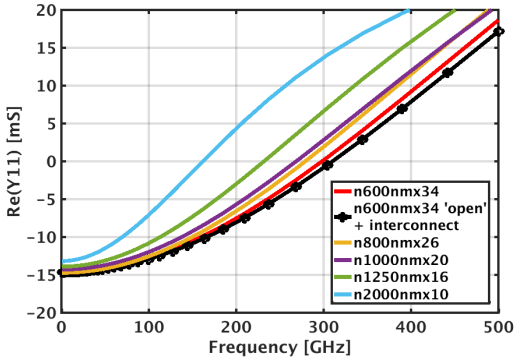
Figure 4.35: 3D view of the 28nm VCO core (a) and side view of the inductor lead connection (b)

together (metal layers 7 to 9, Figure 4.35b), which improves the quality factor of the inductor and compensates for the lack of UTM.

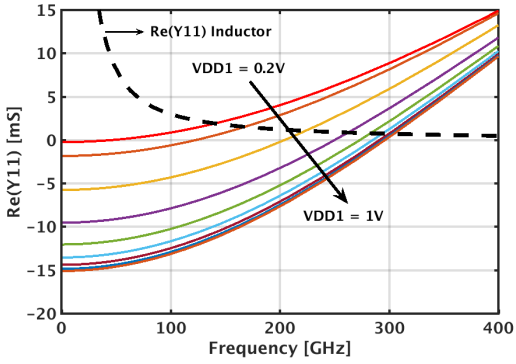
To quantify the potential of the designed transistors for use in a cross-coupled pair VCO, Figure 4.36a presents the simulated Y_{11} for different transistor dimensions. As concluded earlier, a minimal finger width of 600nm yields the highest negative resistance at 215GHz due to the dominance of R_g. Utilizing minimal-length transistors with $F = 34$ and $W = 600$nm, the f_{gm} of the cross-coupled pair reaches as high as 310.15GHz with a $Re(Y_{11}) = -7.1$mS. In Figure 4.36b, the same cross-coupled pair is shown under different supply voltage biases. The black dotted line is the real part of the Y_{11} of the core inductor, which the cross-coupled pair should compensate for to sustain oscillation. As can be seen in the graph, the generated negative resistance becomes larger for increasing supply voltage, which corresponds to a larger current flowing throught the cross-coupled pair. For low supply voltage, the cross-coupled pair cannot generate enough negative resistance to counter the losses of the tank and oscillation is not possible. Starting between 0.4-0.5V, the negative resistance overtakes the losses of the tank and stable oscillation can be maintained.

In order to achieve this high fundamental oscillation frequency, the tank consists of the parasitic capacitance from the cross-coupled and amplifier transistors and the tank inductor (L_{Ind}). No varactors are used, as they would increase the total tank capacitance (reducing the oscillation frequency) and their low quality factor at high frequencies would degrade the oscillation capabilities. Since the main capacitor in the tank is contributed by the cross-coupled pair, Figure 4.36c shows this parasitic capacitance in function of the supply voltage. This variable parasitic capacitance can be used as a tuning mechanism by modifying the supply voltage VDD1 of the VCO core.

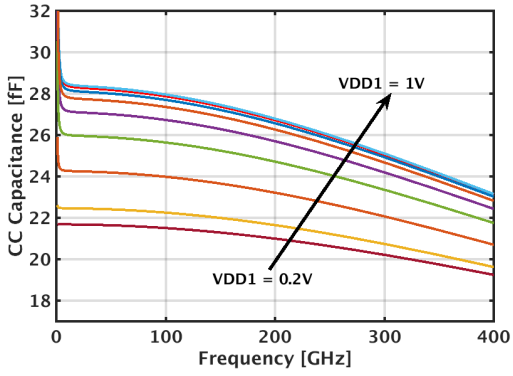
Both the VCO and amplifier were optimized for their required sub-THz functionality: by separating the fundamental generation to the VCO and third harmonic generation to the amplifier, both functions can be optimized separately. The amplifier that generates the wanted above-f_{max} third harmonic acts as a buffer between the VCO core and the antenna. To improve the generation of this third harmonic, the transistors should be operating in the weak-inversion operation region where they show the highest nonlinear behavior. Since the supply voltage of the oscillator core determines the gate-source voltage biasing of the amplifier transistors, ultra-high ultra-low VT (UHVT) transistors are used to enhance nonlinear behavior of the amplifier. The amplifier size is kept small to minimize the capacitive contribution to the oscillator tank, which would lower the oscillation frequency.



(a)



(b)



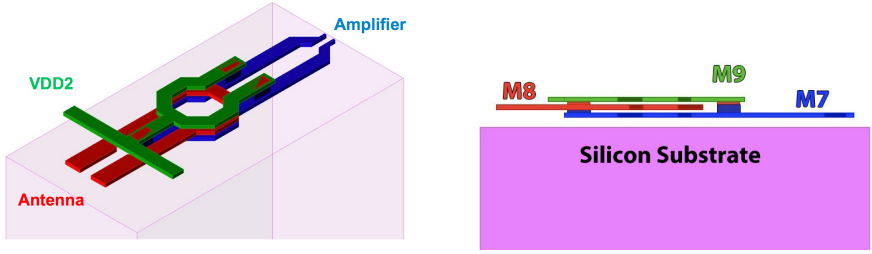
(c)

Figure 4.36: Generated negative resistance by a cross-coupled pair for different finger widths (a), and the resulting negative resistance (b) and parasitic capacitance (c) depending on VDD1 bias

4.4.3 Antenna and output design

Source with collinear dipole and transformer

To emit the generated sub-millimeter waves, the first signal source couples the third harmonic signal from the amplifier to the on-chip antenna through an integrated transformer (Figure 4.37). To push the boundaries of frequencies generated in CMOS, the top frequency is 650GHz. Implementing a transformer with a self-resonant frequency above 600GHz would require very small trace widths and winding diameter, resulting in low signal coupling towards the antenna. Therefore, a transformer is used where the SRF is positioned between the fundamental (ω_0) and third harmonic ($3\omega_0$). The resulting transformer behavior differs for these two frequencies of interest: at ω_0, the transformer impedance is inductive and works towards compensating the output capacitance of the amplifier. At $3\omega_0$, the structure couples the wanted third harmonic to the antenna while having a capacitive impedance, as this frequency is above the SRF of the transformer's inductors.

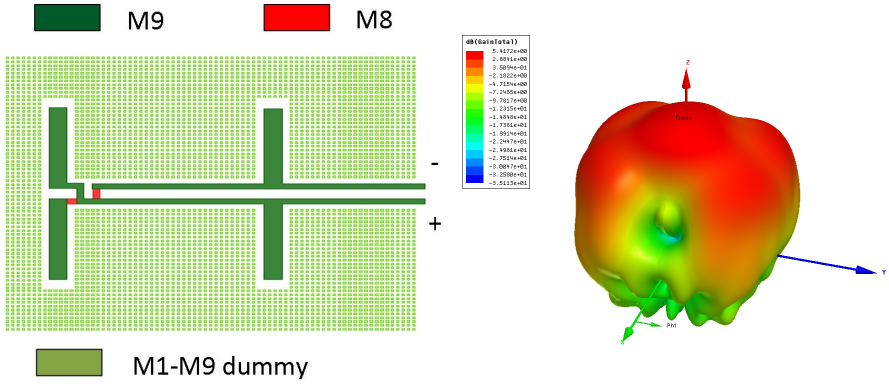


(a) (b)

Figure 4.37: Layout model of the transformer used to transfer the THz signal to the antenna

While using a transformer with a SRF below the target third harmonic frequency would mean that the input impedance would be capacitive, this does not mean that the transformer no longer works above this frequency. This just means that the impedance will change from being inductive to being capacitive, which may complicate some matching properties of the transformer. When evaluating th G_{max} of the transformer, we can see that the insertion loss of the transformer keeps decreasing with frequency and continues beyond the SRF. This low insertion loss, however, is only attainable when both input and output are perfectly matched, where the transformer would like a inductive input and output load. While the impedance of the antenna is inductive, the output impedance of the non-linear amplifier is capacitive. An inductor or transmission line can be placed between the non-linear amplifier and the transformer to match them together, but this matching circuit would also add losses which could be larger than any mismatch losses that would occur if no matching network was used. The transformer

is implemented as three stacked, single-turn inductors in the top three metals with the middle inductor leading to the antenna load. Biasing of the amplifier's transistors is done through the center tap of the transformer winding.



(a) (b)

Figure 4.38: Collinear dipole layout (including dummy metals) (a) and simulated radiation pattern (b)

As mentioned before, the tank inductor is implemented by combining the three top metals in parallel to reduce the series resistance of the inductor. In this design, the inductor consists of a 4µm wide metal trace with a radius of 11µm, resulting in an inductance of 18pH at 215GHz with a simulated quality factor of 36.7 (and a $Re(Y_{11}) = 1.12\text{mS}$).

The antenna is an on-chip collinear broadside dipole (Figure 4.38), implemented in the top metal layer. The antenna is driven differentially by the uneven harmonics, resulting in a suppression of the second and fourth harmonic. The collinear broadside dipole can be considered as a 2x1 dipole array, where the distance between both elements of the array is $\lambda/2$. The signal feed line goes through the first dipole, and crosses right before arriving at the second dipole. The strict dummy metal density requirements should also be met for the antenna, and are included in the layout shown in Figure 4.38a. The radiation pattern at 650GHz can be seen in Figure 4.38b. By using a metal reflector on the backside of the silicon die (on the mounting board), the backside radiation is eliminated and the reflected signal will constructively interfere with the topside radiation. The simulated directivity is 8.7dB (9.3dB at a 14°angle) with a simulated radiation efficiency of 38.7%, resulting in a simulated antenna gain of 4.9dB (5.2dB at 14°) in the Z-direction.

THz source with folded dipole

A second signal source was implemented using an alternative approach for the connection between the output transistors and the antenna by removing the transformer and connect the amplifier directly to the antenna (Figure 4.39). To be able to provide the DC bias to the transistors, the two ends of a dipole antenna are 'folded' together to realize a folded dipole (Figure 4.40). Besides acting as a DC bias to the amplifier, the folded dipole antenna also has a role to fulfill at both the fundamental and third harmonic frequency. The antenna is dimensioned to radiate at the third harmonic, as this is the frequency with the wanted signal. At the same time, the folded dipole will act as a large inductor at the fundamental with a center DC feed tap, eliminating the need for RF choke inductors.

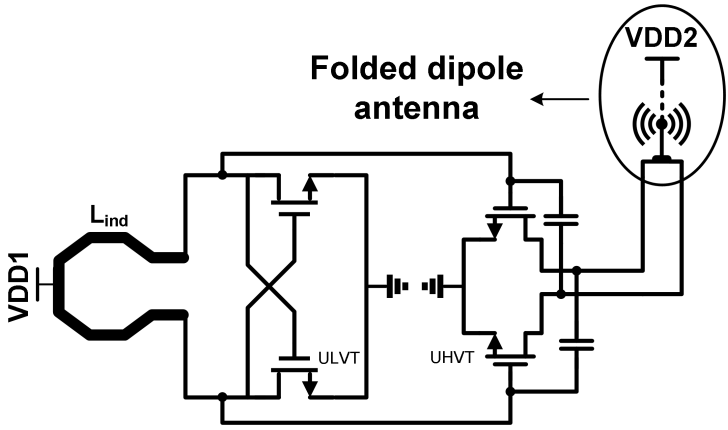


Figure 4.39: Schematic of the 28nm CMOS transmitter with integrated folded dipole

The target frequency is slightly lowered compared to the source with collinear dipole antenna, as the aim of this design was to generate more power. Therefore, the inductor used in the VCO is slightly larger (radius of 12μm instead of 11μm, resulting in an inductance of 19pH with a quality factor of 40.4. The simulated oscillation frequency is 630GHz.

Figure 4.41a shows the layout of the folded dipole with the surrounding dummy metals, as well as the simulated radiation pattern at 630GHz (Figure 4.41b). As is the case with the collinear dipole, a metal reflector plane is placed on the mounting board, under the silicon die. The simulated directivity is 9.2dB with an efficiency of 23.9%, with an antenna gain of 3dB in the Z-direction.

The circuits and antennas are fully compliant with all strict layout rules of the 28nm bulk CMOS process, with manually placed dummy metals near the oscillator core and

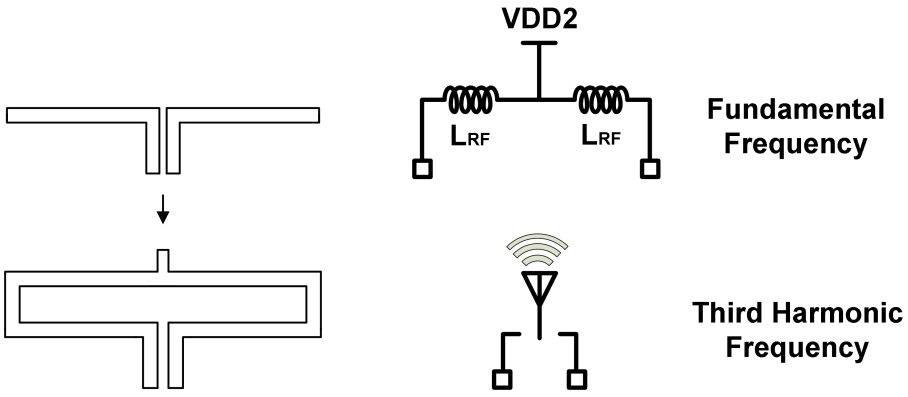


Figure 4.40: Folding of a dipole antenna (a), and its behavior at the fundamental and third harmonic frequency (b)

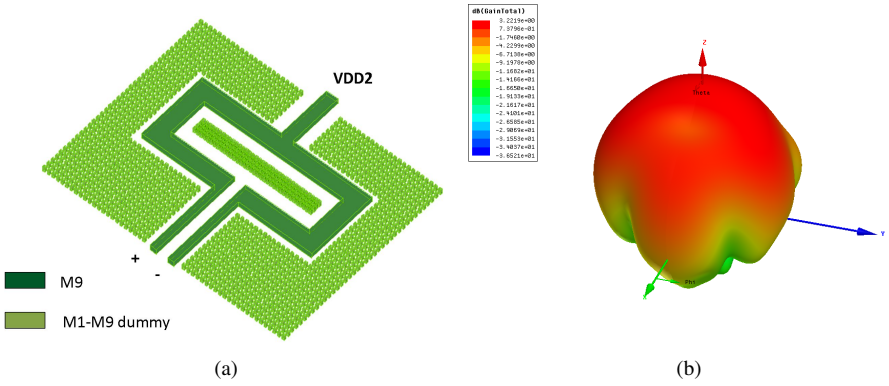


Figure 4.41: On-chip folded dipole layout (a) and simulated radiation pattern (b)

antennas to meet metal density requirements to minimize any negative impact on the circuit's behavior. Figure C.5 shows the 3D simulation models of the collinear and folded dipole, both with and without adjacent metal planes representing the dummy metals surrounding the antennas.

4.4.4 Measurement results

In the measurement setup of this work, the radiated signal was measured with a WR1.5 horn antenna connected to a VDI WR1.5 MixAMC module at a distance of 20mm to satisfy far-field criteria. A baseband amplifier amplifies the down-converted signal before being analyzed by a R&S FSU spectrum analyzer (Figure 4.42). To accurately verify the power levels from the spectrum analyzer, the receiver setup was calibrated using an Erickson PM4 power meter and a VDI WR1.5 source module. The resulting measured frequencies and equivalent isotropically radiated power (EIRP), calculated using Friis' equation, are shown in Figure 4.43 for a varying supply voltage (used for frequency tuning).

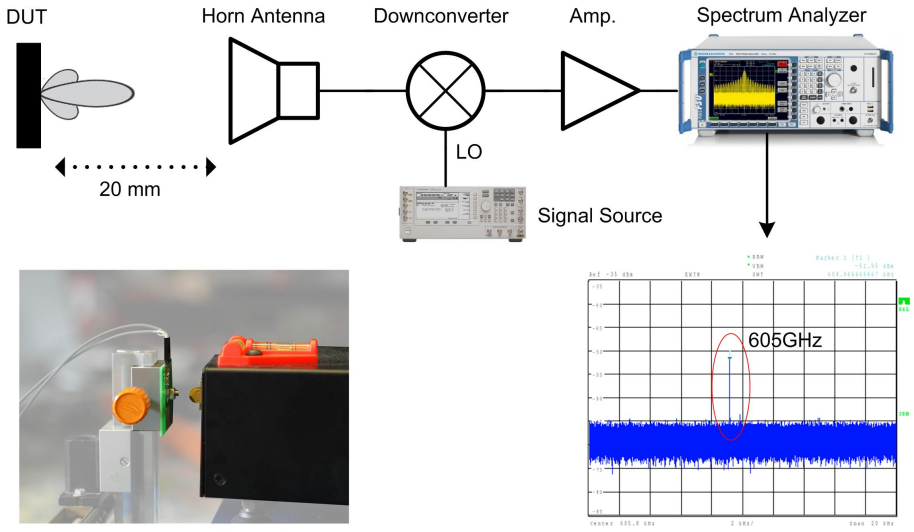
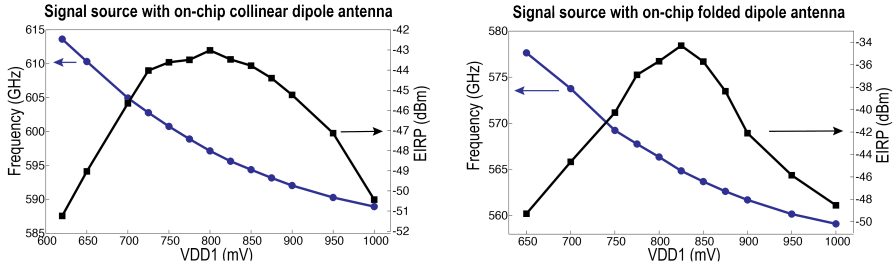


Figure 4.42: Measurement setup and sample output spectrum when measuring the radiation of the 28nm CMOS chips

For the first design, with transformer and collinear dipole antenna, the frequency tuning range is 24.7GHz (588.9-613.6GHz) and the 3dB output power bandwidth is 14.25GHz. The peak measured EIRP is -43dBm for a DC power consumption of 21.2mW. The



(a) (b)

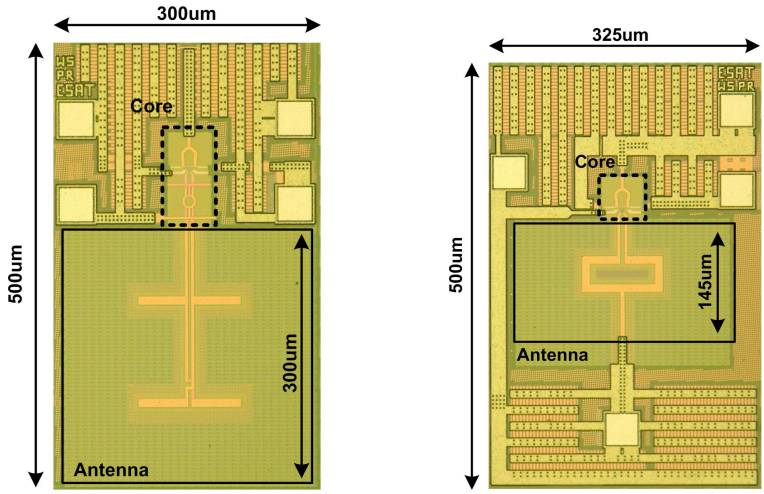
Figure 4.43: Measured EIRP and frequency for the 600GHz (a) and 570GHz (b) signal sources. The supply voltage of the VCO core is changed to vary the oscillation frequency

core and total area (including bond pads and decoupling capacitors) are 50µm x 110µm and 300µm x 500µm, respectively. The folded-dipole approach radiates signals from 559.1GHz to 577.6GHz (18.5GHz tuning range) and has a peak EIRP of -34.3dBm for 21.4mW of DC power. The 3dB output power bandwidth is 4.92GHz and the core and total area are 50µm x 45µm and 325µm x 500µm, respectively.

Die photographs of the transmitter with folded dipole and with collinear dipole antenna are shown in Figure 4.44.

When comparing the measured results with the original simulations, a shift in frequency and output power can be seen. The 600GHz source would oscillate at 650GHz in simulation, while the 570GHz source oscillates at 630GHz in simulation. Besides the implications on the matching of the different components, there is also a large impact on the antenna behavior.

Both collinear dipole and folded dipole were designed to be used with a metal plane reflector at the bottom of the silicon die, located on the mounting board. While this would increase the directivity of the antennas due to the constructive interference at the chosen frequencies, this is no longer the case after the frequency shift: as the frequency shifts, so does the optimal antenna-reflector distance required to achieve constructive interference (total wave travel length should be an uneven multiple of $\lambda/2$). This was most clearly noticeable in the case of the collinear dipole: at 650GHz, the wave travel distance in the 305µm silicon die equaled 9 times $\lambda/2$, while at 600GHz this was changed to 8.2 times $\lambda/2$. Consequently, instead of creating positive interference, the metal reflector caused destructive interference. Therefore, the chip was mounted on a PCB without a metal plane under the die. The comparison between the simulated radiation patterns for the same collinear dipole antenna at 650GHz and 600GHz, resp. with and without the bottom metal reflector, is included in Appendix C.6. The

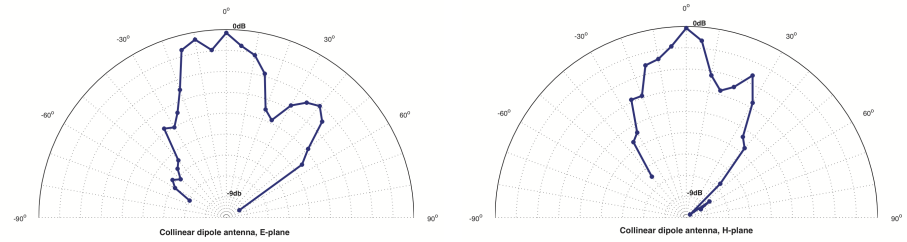


(a) (b)

Figure 4.44: Die photographs of the realized THz sources with collinear dipole antenna (a) and with folded dipole antenna (b)

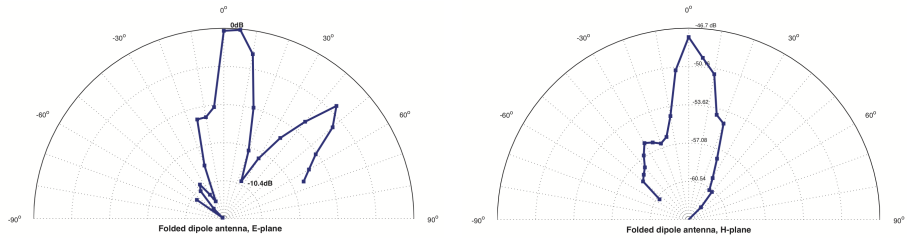
simulated directivity is 5.1dB, antenna gain is 1.5dB and the radiation efficiency is 44%, which includes the radiated energy towards the backside of the silicon die towards the unwanted direction. For the case of the folded dipole, measurements including the metal reflector resulted in slightly more radiated power than without the metal reflector. However, the antenna performance degraded due to the frequency shift from the target 630GHz to 570GHz, as illustrated in Appendix C.7. The simulated peak directivity at 570GHz is 5.4db (at a 12°angle) with a radiation efficiency of 14%, resulting in a simulated antenna gain of -4dB.

The measured radiation pattern of the 600GHz source with on-chip collinear dipole antenna is given in Figure 4.45. Likewise, Figure 4.46 shows the measured radiation pattern of the 570GHz source with on-chip folded dipole antenna, including metal reflector. These radiation patterns carry much more resemblance with their frequency-shifted simulations than the simulated patterns of their original target frequency (Appendices C.6 and C.7). Using the measured EIRP values and the simulated antenna parameters, we can estimate the total radiated power ($TRP = EIRP - D$) and the power delivered by the THz sources to their respective on-chip antennas ($P_T = EIRP - G$). For the 570GHz source with folded dipole, the estimated output power P_T of the source delivered to the antenna is -30.3dBm and a TRP of -39.7dBm due to the low radiation efficiency. The 600GHz signal source with collinear dipole antenna has an estimated P_T of -44.5dBm and TRP of -48.1dBm.



(a) (b)

Figure 4.45: Measured radiation pattern of the collinear dipole THz source at 600GHz (left: E-plane, right: H-plane)



(a) (b)

Figure 4.46: Measured radiation pattern of the folded dipole THz source at 570GHz (left: E-plane, right: H-plane)

4.4.5 THz Non-Destructive Quality Control

One of the possible applications to benefit from fully integrated CMOS imagers is the non-destructive testing of various industrial and consumer products. To illustrate the potential of lens-free THz CMOS imaging, the fabricated signal sources are used as transmitter in a setup for the contact-less, non-destructive quality control of a 21G hypodermic needle (0.8mm diameter, 40mm long) inside their protective plastic casing (5.5mm diameter). The sample-under-test is placed in a setup similar to Figure 4.42 to create a 1-pixel imaging system, which measures the power transmission at a specific point of the scanned object. A mechanical stepper moves the sample in the vertical direction in steps of 0.1mm, thus creating a cross-section image of the received power. The metallic needle will prevent the transmission of the THz waves, and thus will cause a lower received power when it is moved in front of the transmitter. By repeating this line scan at different positions, the position of the needle inside the protective casing can be monitored along the sample's length (Figure 4.47).

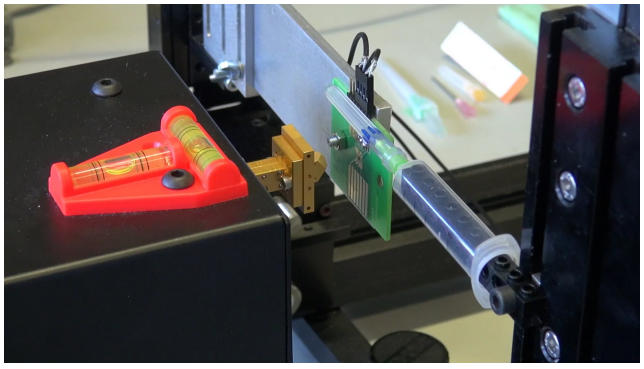


Figure 4.47: Mechanical stepper setup for scanning objects. Image shows a non-destructive testing of a surgical needle using a THz tansmitter

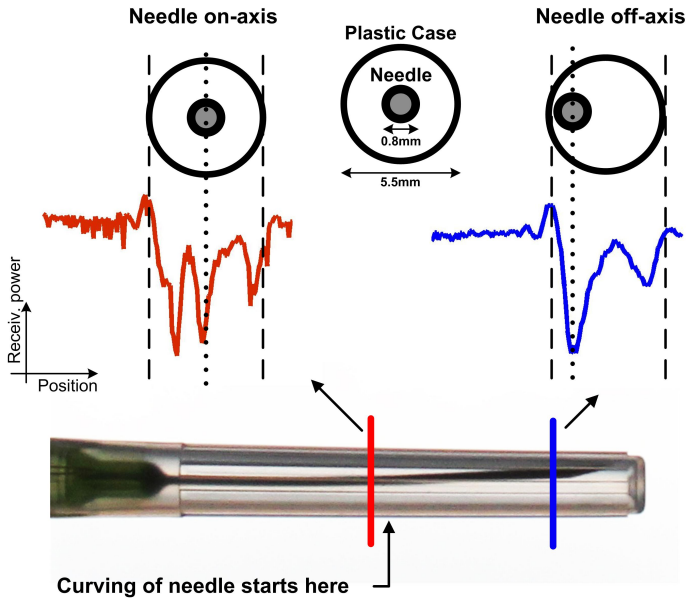


Figure 4.48: Analysis of needle cross-section by measuring the transmitted THz power through the needle case at different points along the needle

The resulting THz cross-sections of the needle-under-test are shown in Figure 4.48. If both the top and bottom end cross-section show a centered needle, the needle is straight and is correctly positioned inside the package. A non-centered position of the needle at the top compared to the bottom indicates a sample that is curved and therefore does not correspond to quality specifications. Possible causes are needle production error or collision of the needle tip with the inner wall of the casing while being assembled, which might results in needle tip damage and a reduced sharpness.

4.5 Comparison with state-of-the-art

Table 4.1 compares the results with current state-of-the-art THz oscillators. The total tuning range and 3dB output bandwidth of the presented chips are the largest reported for bulk CMOS oscillators above 400GHz. The output power and EIRP of >500GHz CMOS signal generators is low compared to recent advancements in the 250-300GHz range. This work shows that despite this power gap, small and cheap CMOS transmitters for lens-free THz imaging are possible and can be used for a variety of (industrial) applications. Fully integrated systems containing transmitters, receivers and signal processing blocks will allow THz applications to be available for consumer products and unleash the full potential of the THz spectrum.

Compared to the work shown in the table, the presented sources are the highest radiating THz sources in CMOS and the first to be implemented in a 28nm bluk CMOS process. The signal sources exhibit a wide tuning range and 3dB output power bandwidth while maintaining a compact layout footprint with on-chip antenna. The circuits are used as THz transmitters in a measurement setup for the contactless, non-destructive testing of hypodermic needles inside their protective casing. A lens-less, fully integratable CMOS imaging system with high- pixel density could enable the widespread use of THz imaging as a cost-effective solution for non-destructive quality control, both for industrial and consumer applications.

Figure 4.49 plots the output power of current state-of-the-art radiating transmitters above 200GHz. While this graph ignores other design parameters (tuning range, area, power consumption,...), some clear trends can be observed: The first trend is to push towards higher frequency, where the output power of a single radiating cell is limited. This work demonstrated the highest frequency in CMOS, without the use of a lens or special packaging requirements. The second trend is combining different radiating cells into arrays. This is very clear at the high end of the mm-wave spectrum (250-350GHz), where research activity in the past years has pushed towards coupling many signal generator cores together, breaching the 0dBm output power limit.

4.6 Conclusion on THz transmitters

In this chapter, a 0.54THz signal generator fabricated in 40nm bulk CMOS is presented which generates and extracts the third harmonic from a 180GHz LC-VCO using respectively a buffer and transformer. Frequency tuning is realized by parasitic I-MOS varactors present in the VCO transistors. Two versions of this signal generator are presented and discussed: one with probe pads, and one with an on-chip planar antenna. On-wafer measurements show a 21.9GHz tuning range (539.6GHz to 561.5GHz) and 3dB output bandwidth of 5.5GHz (539.6GHz to 545.1GHz), which are the widest ranges for CMOS signal generators above 400GHz. The measured peak output power is -31dBm at 543GHz, for a DC power consumption of 16.8mW. The same signal generator was also fabricated with an on-chip planar dipole antenna. A metal plane on the substrate bottom is used to improve the radiation efficiency by reflecting substrate waves to create constructive interference at broadside. The transmitter with antenna is used in a lens-free THz imaging setup, resulting in the dielectric contrast images shown. This chapter demonstrates the feasibility of a low-cost CMOS THz imaging transmitters without bulky and expensive substrate or beam-focusing lenses.

Table 4.1: Comparison with state-of-the-art signal generators above 400GHz

Ref.	Frequency (GHz)	Tuning Range (GHz)	Output Power (dBm)	EIRP (dBm)	DC power (mW)	Area (mm^2)	Process Technology
[Seo10a]	410	3	-49	-	16.5	0.25	45nm CMOS
[Pfe14]	530	17	-11.3	25*	150	0.26	130nm SiGe
[Zha16a]	541	21	-27*	-	172	2.8	65nm CMOS
Probe	**539.6-561.5**	**22**	**-31†**	**-**	**16.8**	**0.051#/0.15**	**40nm CMOS**
Dipole	**538.4-549.7**	**11****	**-33.55**	**-31.8**	**18.9**	**0.033#/0.15**	**40nm CMOS**
[Shi11]	553	< 1	-36.6	-	64	0.29	45nm CMOS
Folded Dipole	**559.1-577.6**	**18.5**	**-30.3**	**-34.3**	**21.4**	**0.00225#/0.16**	**28nm CMOS**
Collinear Dipole	**588.9-613.6**	**24.7**	**-44.5**	**-43**	**21.2**	**0.0055#/0.15**	**28nm CMOS**

* Uses a hemispherical lens

† Measured on version with probe

** Limited by equipment noise floor

Active/core area

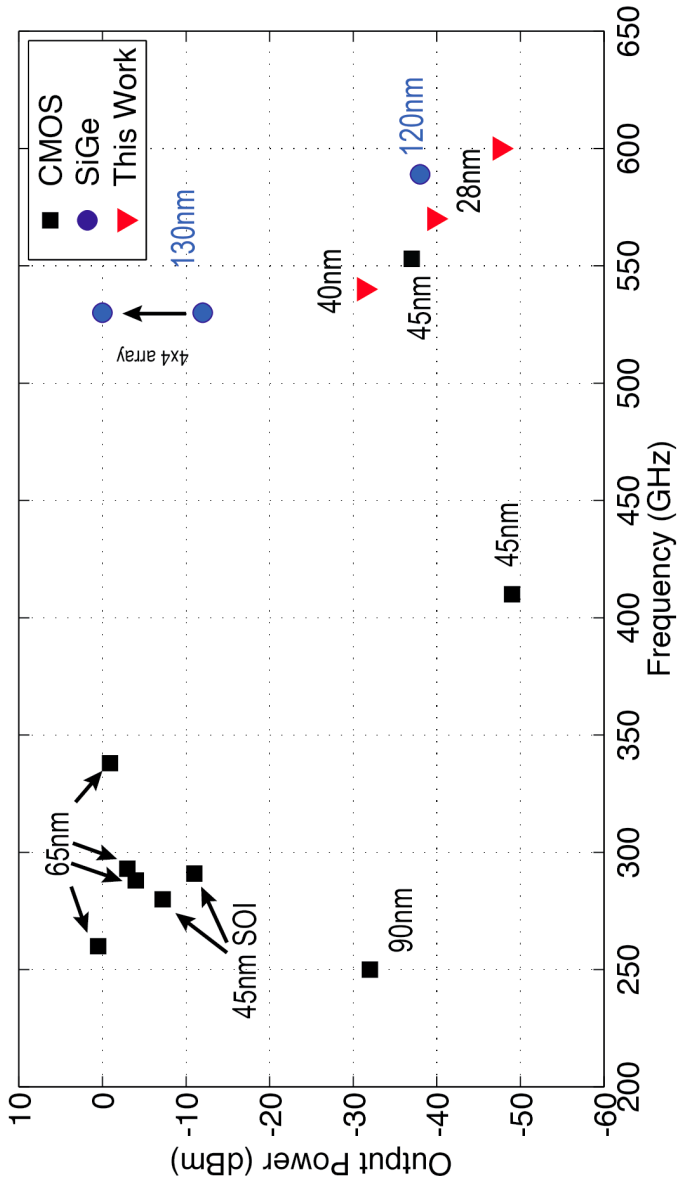


Figure 4.49: Overview of state-of-the-art radiating transmitters with their radiated output power versus frequency

Table 4.2: Overview of state-of-the-art signal generators above 200GHz

Probe/Antenna	Frequency (GHz)	Tuning Range (GHz)	Output Power (dBm)	EIRP (dBm)	DC power (mW)	Area (mm^2)	Process Technology	Ref.
Probe	573	< 1	-19.2	NA	115	0.41	0.25µm InP HBT	[Seo11]
Probe	482	NA	-7.9	NA	61	0.02**	65nm CMOS	[Mom11]
Probe/Antenna#	288	4	-1.5/-4.1	-	280	0.29	65nm CMOS	[Grz13]
Probe	324	4	-46	NA	12	0.038	90nm CMOS	[Hua08]
Antenna array*	280	9	-7.2	9.4	820	7.3	45nm SOI	[Sen12]
Antenna array#	260	3.7	0.5	15.7	800	2.3	65nm CMOS	[Han13c]
Patch Antenna	589	-	-38	-	14	0.47	120nm SiGe	[Seo10b]
Patch array	338	2	-0.9	17	1540	3.9	65nm CMOS	[Tou15]
Antenna	380	15	-17.3	-11	380	4.18	130nm SiGe	[Par12]

* Wafer-thinning

Uses a hemispherical lens

** DC power supply through probe, no bond pads

Chapter 5

THz receiver circuits

5.1 THz receiver introduction

After a THz signal has been generated, a receiver circuit is required to capture the signal and demodulate the transmitted data or analyze the received signal properties when used in an imaging system. THz receivers are notoriously difficult to implement due to two major issues:

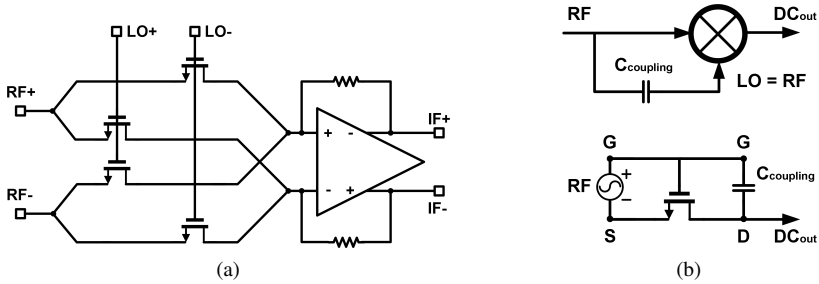
- The input signal strength is low: as discussed in the previous chapter, generating a high power signal at THz frequencies is not easy due to the usage of (low efficiency) harmonic generators. In addition, the free-space path loss drastically attenuates the transmitted signal of wireless systems.
- Where at mm-wave frequencies low-noise amplifiers (LNA) can be used to boost the weak input signal, this is not possible for THz frequencies as the incoming signal is above the transistor's f_{max}. Amplification of the THz signal before being downconverted is not possible, which places stringent requirements on the sensitivity of the receiver.

The following sections will discuss and overview some of the possible receiver topologies, their (dis)advantages and the design of an injection-locked divider, a super-regenerative receiver and a Schottky barrier diode detector.

5.1.1 Resistive downconverters and self-mixing transistors

Even though there is no more gain above f_{max}, mixers/downconverters are still an option [Tyt11] [Gue13]. Without the LNA between the THz input and the mixer, these systems are sometimes referred to as 'mixer-first' architectures. Since the input frequency is beyond the f_{max} of the technology, the transistors behave as variable

resistors and one ends up with resistive or passive mixers [Cro95] (Figure 5.1a). The local oscillator (LO) and THz signal modify the channel resistance of the transistors, which results in a current proportional to the LO and THz signal product. As there is no gain, the conversion gain is negative/the conversion loss is positive.



(a) (b)

Figure 5.1: Dual-balanced resistive mixer (a) and self-mixing transistors (b) used to detect signals above f_{max}

One major drawback of using passive mixers is that they require a large LO power: since the output signal depends on the product of the LO and THz signal, and the input THz signal is small with no pre-amplification possible, the LO power should be increased to compensate the low-power input signal. Depending on the input frequency and the target intermediate frequency (IF), the required LO power might be very difficult to generate: if the receiver should downconvert an above-f_{max} signal to baseband/low IF, the required LO is also above the f_{max} and thus require a harmonic oscillator with sufficient output power [Sha14].

Another option that has been proven at THz frequencies is self-mixing or cold-mixing, where the THz input signal is connected to both the gate and drain of an unbiased ("cold") transistor (Figure 5.1b). The input signal self-mixes [Dya93] [Oje09], and the resulting DC current is proportional to the input power. By placing a high-gain trans-impedance amplifier (TIA) behind the self-mixing transistor, detection of the input power of the THz signal can be implemented [Sch11]. The downside is that due to the self-mixing, there is no frequency selectivity: all frequency signals that enter the receiver self-mix to the same baseband signal. This can be circumvented by modulating the THz signal with a known frequency, and looking for this modulated signal in the detector's output voltage. This energy-detector type of receiver has been successfully used at THz frequencies: 1k-pixel array detectors have been demonstrated [Had12], as well as near-field sensors [Grz16].

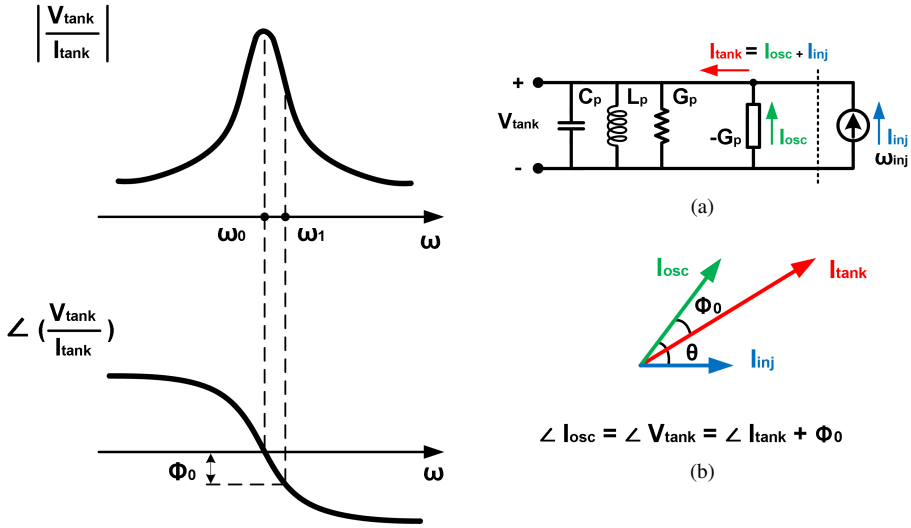


Figure 5.2: Conceptual representation of injection locking of a cross-coupled oscillator, with 1-port tank representation (a) and current phasors (b)

5.1.2 Injection-locked dividers

Injection locking, where a periodic signal is injected into an oscillator, was first studied by Adler [Adl46] and later by Razavi [Raz04]. For a cross-coupled LC oscillator, the tank resonates at frequency ω_0 as long as the total phase shift of the feedback loop remains equal to 360° (Equation 4.3). By adding an additional phase shift ϕ_0 in the feedback loop, the tank can no longer resonate at ω_0 since the total phase shift of the loop at that frequency is now equal to 360° plus ϕ_0 instead of the required 360°. Therefore, the oscillation frequency of the resonator changes to ω_1, as illustrated in Figure 5.2, to accommodate for the added phase shift ϕ_0 and to meet the Barkhausen phase criterion.

One way of introducing this phase shift is by injecting a current I_{inj} with frequency ω_{inj}, as shown in Figure 5.2. As a result, there is an angle θ between the oscillator current I_{osc} and the injected current I_{inj}, such that the tank current I_{tank} realigns with the tank voltage after undergoing the ϕ_0 phase shift at ω_{inj}.

Using this technique, a free-running oscillator operating at ω_0 being injected by a signal ω_{inj} locks to the injected signal and change its oscillation frequency to ω_{inj} as long as ω_{inj} falls within the locking range $\Delta\omega$ of the resonator.

$$\Delta\omega = \omega_0 - \omega_{inj} = \frac{\omega_0}{2 \cdot Q_{tank}} \cdot \frac{I_{inj}}{I_{osc}} \tag{5.1}$$

From Equation 5.1 [Raz04] one can conclude that to maximize the injection locking range, the current of the injected signal I_{ing} should be large. In addition, a high quality factor Q_{tank} reduces the locking range: a resonator with a very high Q is very frequency selective and has a very steep phase characteristic, and thus only oscillates at (or very close to) the free-running frequency ω_0. Decreasing the quality factor of the tank facilitates the deviation of the tank frequency and consequently the locking of the oscillator to the injected frequency. One must of course be careful not to degrade the quality factor too much, as this increases the negative-resistance requirements for the cross-coupled transistor pair to ensure oscillation start-up.

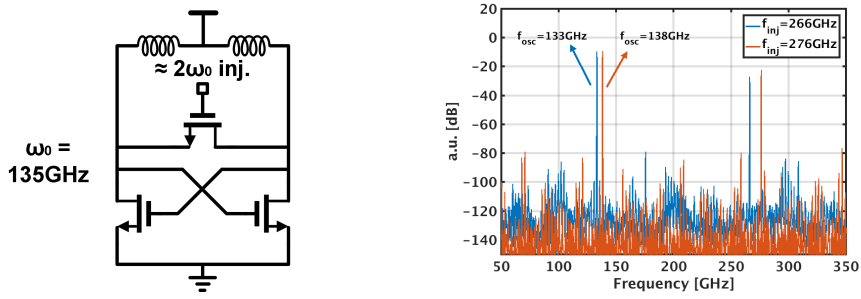
By evaluating the oscillation frequency of the resonator, one can detect if there is an injecting signal present. This can be expanded to the detection of higher-order harmonics by injecting the harmonic signals in the resonator tank and monitoring the fundamental frequency. This type of circuits are called injection-locked dividers, as they divide the input signal down to a multiple of the input frequency.

The injection locking technique was studied for its potential application in detecting THz signals. Two different topologies are investigated: a divide-by-2 and divide-by-3 injection-locking divider, which should lock on input frequencies close to respectively the second and third harmonic of the free-running oscillator frequency ω_0. The oscillator core is based on the 180GHz VCO core from Section 4.3, but the addition of the injection transistors adds their parasitic capacitances to the tank, and results in a decrease of the fundamental oscillation frequency.

The divide-by-2 detector is shown in Figure 5.3a, where the second harmonic is injected through a transistor switch between the two nodes of the cross-coupled VCO. The cross-coupled transistors acts as a mixer for the incoming signal, resulting in $\omega_0 \pm \omega_{inj}$ components. The sum component is suppressed by the resonator tank selectivity, while the difference component acts as the injecting signal [Raz04]. Another way of understanding the dividing operation of this topology is that the injecting transistor acts like a switch between the two oscillator nodes. When the device turns on, this creates a low-impedance path between the two nodes which forces their voltages to become equal. As the input frequency is (close to) twice that of the oscillator frequency, this "forces" the crossing time of the differential signal to synchronize to the injected frequency ω_{inj} [Gu11].

The cross-coupled pair consists of two 28µm/40nm NMOS transistors, and the injection switch is a 30µm/40nm NMOS transistor. The free-running frequency ω_0 is equal to 135GHz with $2\omega_0$ being 270GHz. Figure 5.3b shows the spectrum of the oscillator signal when being injected with a signal ω_{inj} equal to 266GHz and 276GHz with a P_{inj} of 1.9dBm: the oscillator locks onto the harmonic injector, and the fundamental

oscillation frequency is pulled away from the free-running 135GHz to $\omega_{inj/2}$ (133GHz and 138GHz, respectively). The total locking range is 10GHz and the locking input frequency ranges from 266GHz to 276GHz. Injected signals with a frequency outside this locking range do not pull the oscillator away from its free-running frequency: the output spectrum contains both a peak at 135GHz (free-running) and at $\omega_{inj}/2$, indicating that injection-locking was not successful.



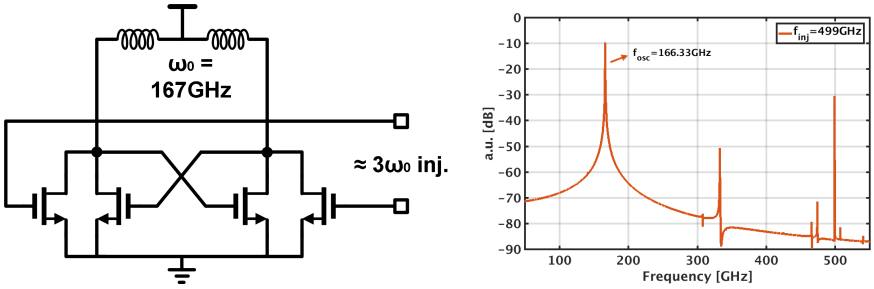
(a) (b)

Figure 5.3: Schematic of a divide-by-2 injection-locking divider (a) to detect a ≈270GHz signal, with its signal spectrum and locking range shown in (b)

To increase the frequency of the input signals that can be detected up to 500GHz, a divide-by-3 detector is designed where the ω_{inj} approximates the third harmonic of the VCO, and is injected through two injection transistors (Figure 5.4a). The cross-coupled pair and injection transistors have the same transistor dimensions (22µm/40nm NMOS transistors) and result in a free-running frequency ω_0 equal to 167GHz with a $3\omega_0$ of 501GHz. The injected current in the tank is low, as the 500GHz injection signal is far beyond the f_{max} frequency of the 40nm CMOS technology. Consequently, with a large input power P_{inj} of 1.3dBm, the locking range only ranges from 499GHz to 501GHz. In Figure 5.4b, the oscillator signal spectrum shows the oscillator frequency successfully being pulled away from the 167GHz free-running frequency to 166.33GHz.

The main obstacle for THz injection-locking receivers is that it requires a high-power THz signal to pull the oscillator away from its free-running frequency and lock to the nth harmonic of the THz signal. From Equation 5.1, the current ratio I_{inj}/I_{osc} requires a very large I_{inj} which is very difficult to achieve at THz frequencies. Another approach could be to reduce the oscillation current I_{osc} or the quality factor of the tank to facilitate locking, which increases tank losses, the necessary compensation by active circuits and thus an increase in transistor size/reduction in oscillation frequency.

The requirements of high input power for a medium locking range [Gu11] or very limited locking range for medium input power [Lin10] can also be found in literature.



(a) (b)

Figure 5.4: Schematic of a divide-by-3 injection-locking divider (a) to detect a ≈500GHz signal, with the spectrum of the oscillator locked onto a 499GHz input signal shown in (b)

While measurement equipment and on-wafer probes can deliver input power of up to 0dBm at 300GHz, this is not yet possible at 500GHz and above. In addition, when the injection-locked receiver is to be used in a wireless communication or imaging application, the free-space path loss drastically attenuates the output power generated by the THz transmitter, which places an unachievable burden of required generated output power by the transmitter.

5.2 Fully integrated THz super-regenerative receiver with downconverter

While injection-locking a free-running oscillator with THz signals proves to be very difficult, the idea of injecting a signal into a resonator tank to change its behavior remains interesting. In the previous section, it was found that trying to alter an oscillator running in steady-state is difficult without sufficient input power. However, when the oscillator is starting up, there is a window of opportunity to influence the resonator's start-up characteristics with even a small injection signal. By evaluating this start-up behavior using an envelope detector, information about the input signal strength can be deducted. This type of receiver was first presented in 1922 by Edwin H. Armstrong [Arm22] and is called the Super-Regenerative Receiver (SRR), whose concept and implementation to detect THz signals in CMOS are discussed in this section.

5.2.1 SRR concept

Oscillators operating in steady-state exhibit a stable oscillation with a constant amplitude of the oscillation voltage and envelope. However, before they reach this steady-state operation, the oscillator goes through a very non-linear, transient start-up phase. It is this start-up behavior that forms the core of the SRR operation.

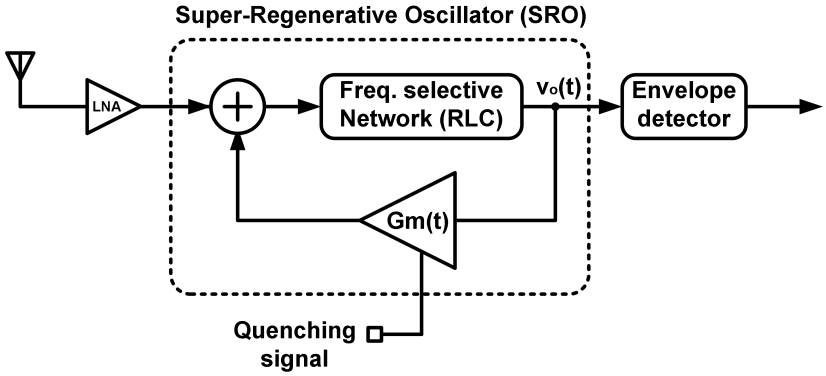


Figure 5.5: Conceptual representation of the SRR operation

Figure 5.5 shows a block diagram representation of the SRR [MG05]. At the heart is the super-regenerative oscillator, which can be represented by a frequency-selective network (formed by the RLC network that forms the resonator tank) and a quenchable variable-gain amplifier (VGA) feeding the output signal back to build up oscillation. In normal oscillator start-up, this feedback gain decreases with increasing output voltage until the loop gain becomes unity and steady-state oscillation is achieved (Section 4.1). For the case of a SRO, the VGA gain is further modified by a periodic quenching signal Q, which makes the feedback loop periodically meet and fail the Barkhausen criteria. Therefore, the oscillator repeatedly starts up and fades out. If the oscillator output is connected to an envelope detector that tracks the envelope of the tank voltage, the resulting output is a series of pulses, spaced according to the period of the quenching signal. Each pulse/envelope represents the rise, steady-state and fall of the oscillation of the resonator as the quenching signal reduces and increases the feedback loop gain.

The output voltage waveform for a sinusoidal quenching signal is given in Figure 5.6. If the quenching current i_Q rises above the minimum bias current I_{on} to sustain oscillation, the oscillator attempts to start up. By adding an RF input signal with the same frequency as the oscillation frequency of the resonant tank, the build-up of the oscillation voltage during start-up can be boosted compared to the case where only noise is present at start-up. This leads to two possible modes of operation when utilizing a SRR. The first mode is when the reduction in oscillation start-up time due to the input signal allows

the oscillation to reach a higher peak amplitude before being damped. This is the linear mode, and the difference in peak amplitude is proportional to the amplitude of the signal being injected. The second mode of operation is the logarithmic mode, where the oscillator voltage can reach steady-state and the peak amplitude remains the same. However, as a stronger injected signal helps speed up the start-up of the oscillation more, the total area under the envelope is proportional to the input amplitude. Put in another way, the slope of the oscillation build-up comes earlier for stronger injected signals while dying out at approximately the same time.

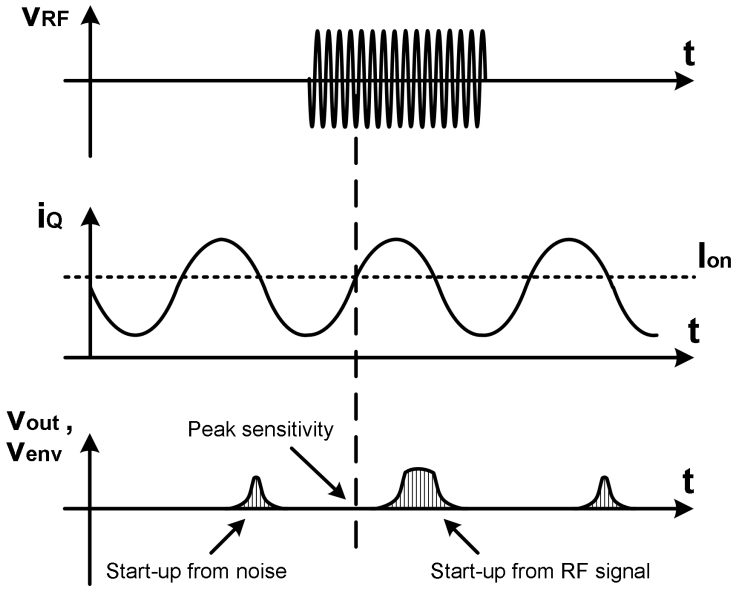


Figure 5.6: RF input, quenching current and SRO output voltage waveforms illustrating the difference in oscillation start-up

One disadvantage of the SRR is that this non-coherent detector does not preserve the phase information of the received signal. This makes it incompatible with the quadrature modulation schemes popular in high-speed communication links, and limits its uses to ASK/OOK communication links, where the SRR topology enables ultra low-power receivers with high sensitivity for battery-limited applications [Boh09a] [Oti05]. The quenching frequency will also limit the data rate that can be received in an SRR-based communication link, as this determines how often the SRR can "sample" the incoming signal amplitude. However, this does not rule out amplitude-based imaging setups, such as the one presented in Section 4.3.4, which require a much lower sampling frequency. The relationship between the output signal and the input power is logarithmic, which can improve the dynamic range of the imaging system [Tan13].

The SRR is most sensitive to the injected input signal at the onset of oscillation, when i_Q is equal to the minimum bias current I_{on}. Referring back to the previous section on injection-locking, this short period of peak sensitivity is where the injected signal is larger than the oscillation signal, and therefore can effectively influence the oscillator behavior. Once the oscillator has started, the situation becomes similar to an oscillator being injected with a very small input signal, meaning that the SRO is not sensitive to the input signal anymore until the next quenching cycle. While the analysis of the strongly non-linear behavior of an oscillator's start-up phase is already quite convoluted, this is further complicated by the quenching signal and the resulting varying damping function during the build-up and fade-out of the oscillation. For a more in-depth and mathematical approach towards super-regenerative receiver theory, the reader is refered to [MG05] and [Boh09b] for resp. time-domain and frequency-domain analysis.

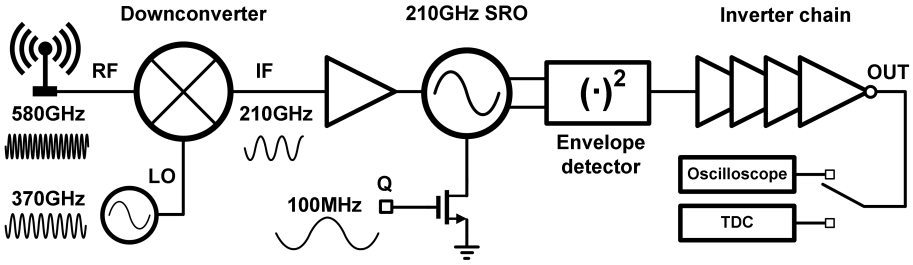
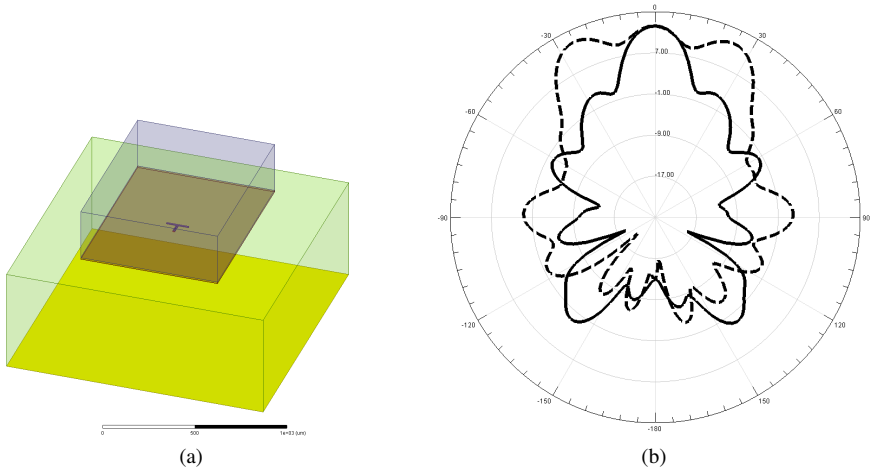


Figure 5.7: Schematic of the proposed THz SRR with downconverter

The high sensitivity to low input power at the edge of start-up makes the SRR an interesting candidate for detecting THz signals. The LNA depicted in Figure 5.5 cannot be implemented for input frequencies higher than the f_{max} of the technology, but can be removed without detrimental effect on the SRR operation. The proposed SRR topology is shown in Figure 5.7: it consists of a mixer-first receiver which downconverts a 580GHz signal, captured by a flipchip dipole antenna, to the 210GHz IF frequency. The downconverter is implemented by a dual-gate mixer, driven by a 370GHz LO signal generated on-chip. The resulting 210GHz IF signal then forms the input signal of a 210GHz SRO, quenched by a 100MHz signal that controls the current through the bias transistor at the bottom of the SRO core. The output voltage of the SRO is subsequently fed to an envelope detector, and the resulting signal is brought off-chip through an inverter driver chain.

5.2.2 Flipchip dipole antenna

To receive the THz signals emitted from the transmitter, the SRR circuit is equipped with an on-chip antenna. A dipole antenna, similar to the one from Section 4.3.2, is implemented. However, the whole die is flipchipped, resulting in the THz signal having to propagate through the silicon substrate to reach the detector. From the previous discussions on on-chip antennas, it was concluded that a large part of the radiated signal of a dipole antenna is being radiated into the substrate instead of towards the air above the silicon die. Part of this substrate radiation could be recovered using a reflector which improves the directivity. This approach still results in a relatively low radiation efficiency. By using flipchip instead of bondwires, the whole die can be rotated and the unwanted substrate radiation becomes the wanted output signal. Thanks to the antenna reciprocity property, this also means that the enhancement of the antenna gain of a flipchip dipole antenna is also true when used as a receiving antenna. Figure 5.8 shows the simulation setup for the flipchip dipole antenna, as well as the improved radiation pattern.



(a) (b)

Figure 5.8: 3D model (a) and simulated directivity (dB) radiation pattern (b) of the flipchip dipole antenna (ϕ angle: dashed = 0°, solid = 90°)

The idea to use a reflector to recover the radiation in the opposite direction of the desired orientation can also be applied when using flipchip: instead of placing the metal plane under the silicon die, as was the case in Sections 4.3 and 4.4, the reflector is placed at the bottom of the PCB board. By making sure that the THz wave travel distance through the PCB material is equal to an uneven multiple of $\lambda/2$, constructive interference improves the radiation performance. Figure 5.9 illustrated this by changing

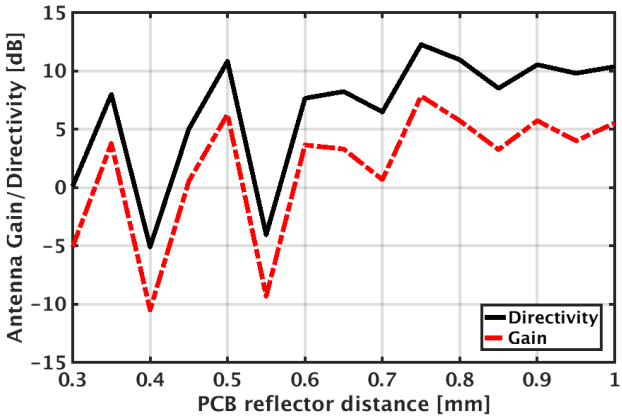


Figure 5.9: Simulated flipchip dipole gain and directivity for varying reflector distance

the PCB material (FR-4) thickness and thus the antenna-reflector distance. From the available PCB thicknesses, a 750µm board ($\approx 11x\lambda/2$) provides a peak directivity of 12.25dB while also maintaining mechanical strength as a chip carrier substrate. The radiation efficiency is 30% and the resulting peak gain is 7.8dB.

5.2.3 Dual-gate mixer

In the classical SRR system, an LNA is placed after the receiving antenna (Figure 5.5) and before the SRO. Since the target frequency is 580GHz, there is no amplification possible due to the limitation of f_{max} and the "A" in LNA would stand for "Attenuator" instead of "Amplifier". Additionally, it is not feasable to create a SRO with a fundamental oscillation frequency of 580GHz (Chapter 4) into which the THz input signal can be injected directly. Implementing a below-f_{max} SRO and use the harmonics of the input signal to trigger the SRO start-up could possibly work but the below-f_{max} harmonic component would only be a small fraction of the incoming THz signal. Therefore, the input power of the above-f_{max} THz signal would need to be very high, which due to the difficulties of generating large output powers and the large attenuation due to FSPL is very challenging.

In this work, this issue is solved by placing a passive mixer in front of the SRO (Figure 5.10). As the input signal strength is already quite low, the LNA was omitted and the input signal from the antenna is connected through a transformer balun to the mixer, creating a mixer-first receiver topology. The mixer downconverts the 580GHz input

signal with a 370GHz LO signal to an IF frequency of 210GHz, which is then fed to the SRO with a fundamental oscillation frequency of 210GHz.

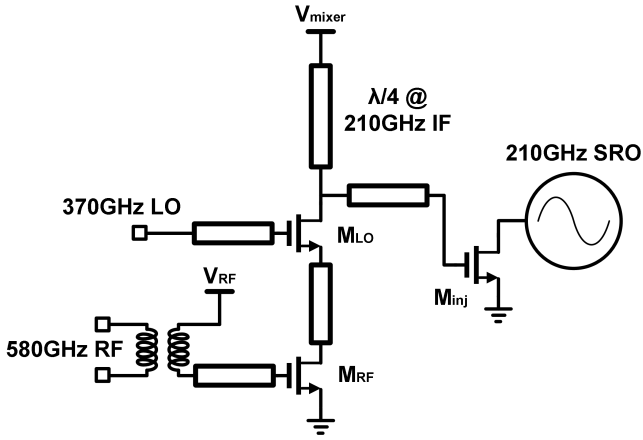
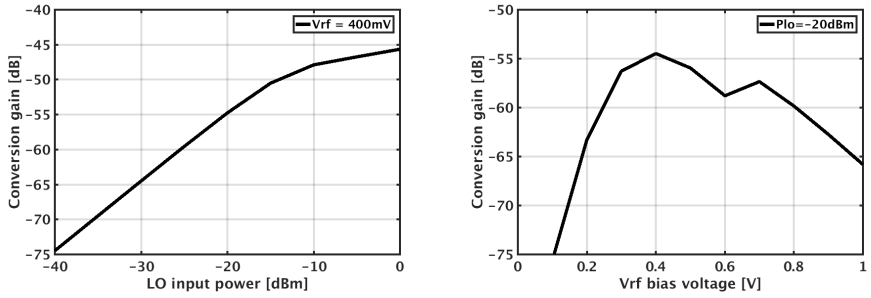


Figure 5.10: Schematic of the dual-gate mixer used to downconvert the incoming THz signal to IF

The dual-gate mixer [Tsi84] [Sul99] consists of two transistors stacked on top of each other, with the bottom transistor M_{RF} having the 580GHz input signal and the top transistor M_{LO} the 370GHz LO signal. In this configuration, M_{RF} is biased in the triode region and acts as the mixer transistor. Meanwhile, M_{LO} is biased in the saturation region to operate as an IF amplifier for the mixing product present at the drain of M_{RF} [Kuo09]. As will be discussed in the next section, the LO signal is generated by a push-push VCO, meaning that this node already carries a high biasing voltage equal to the supply voltage of the LO-VCO (0.8V-1V). The gate biasing of M_{RF} is realized by the input balun. Each interconnection trace is modeled as a transmission line, dimensioned to provide conjugate matching at the relevant frequencies between each component.

The resulting IF signal at the drain of M_{LO} is then injected in the SRO through transistor M_{IF}. A $\lambda/4$ transmission line at the 210GHz IF frequency is placed between the M_{LO} drain and the supply voltage of the mixer, to create a high impedance at IF and steer the IF signal to M_{IF}. Besides injecting the IF signal, M_{inj} also acts as a buffer to isolate the SRO tank from the mixer, which would otherwise increase the tank capacitance and reduce the SRO oscillation frequency. To evaluate the performance of the dual-gate mixer, the power conversion gain is simulated for varying LO driving power and M_{RF} gate biasing voltages, plotted in Figure 5.11. The simulation includes all matching and interconnection losses (RF path: starting from the antenna output, LO path: starting at the center-tap output of the LO-VCO). The conversion gain is the ratio of the 210GHz

IF power delivered to M_{IF} and the 580GHz input power delivered by the antenna. The negative value of the conversion gain indicates that there is a conversion loss, as the dual-gate mixer operates as a passive mixer due to the above-f_{max} frequencies used.



(a) (b)

Figure 5.11: Conversion gain (loss) of the dual-gate mixer depending on P_{LO} (a) and bottom gate bias voltage V_{RF} (b)

As can be concluded from Figure 5.11a, the higher the LO power, the better the conversion gain. This need for high LO driving power is a typical requirement seen in passive mixers and doublers [Tyt11] [Han13a] [Sha14]. For a 370GHz LO power of -20dBm to -10dBm, the conversion gain increases from -54dB to -47dB, with compression of the conversion gain occuring in this input power range. Figure 5.11b shows the conversion gain for varying DC gate bias of the bottom transistor M_{RF}, assuming a -20dBm LO power and the gate of M_{LO} biased at 800mV. Peak conversion gain is attained when M_{RF} is biased at 400mV, confirming the design choice to have M_{RF} operate in triode and M_{LO} in saturation region.

5.2.4 370GHz LO generation

Generating the LO frequency with measurement equipment and bringing this large a signal at 370GHz on-chip would prove to be a challenge (Chapter 3). In addition, the presence of probes and/or the delicate cable connections to the measurement equipment would complicate the usage of the receiver in any imaging setup. Therefore, the LO is generated on-chip.

As the required frequency of the LO is beyond the f_{max}, a harmonic oscillator is required. For simplicity, the choice fell on a push-push VCO where the second harmonic is extracted at the center tap of the tank inductor, as depicted in Figure 5.12a. A $\lambda/4$ transmission line at the second harmonic is added to provide a high impedance towards the DC voltage source, and a transmission line is used to connect the 370GHz

LO signal to the gate of the mixer. Due to the differential nature of the VCO, the fundamental signal at 185GHz cancels at the center tap of the inductor.

The LO-VCO's main goal is to drive the dual-gate mixer and to generate as much LO power at 370GHz as possible to increase the conversion gain (Figure 5.11). Frequency selection of the input THz signal can also be achieved by tuning the LO frequency: as the SRO's tank is only sensitive to an injected IF signal at 210GHz, the detector would be sensitive for any input frequency equal to 210GHz plus the LO frequency. Using parasitic capacitance tuning through the supply voltage of the LO-VCO, VDD2, the LO frequency and output power can be modified (Figure 5.12b). Using a 1V supply voltage, the generated LO power is -12.7dBm at 370GHz. 0dBm fundamental power is generated in the LO-VCO core, of which -25dBm reaches the mixer. The LO frequency tuning range extends from 370GHz to 384GHz. As discussed in the section on the dual-gate mixer, the chosen supply voltage of the push-push VCO also determines the gate bias voltage of transistor M_{LO}, which should operate in the saturation region.

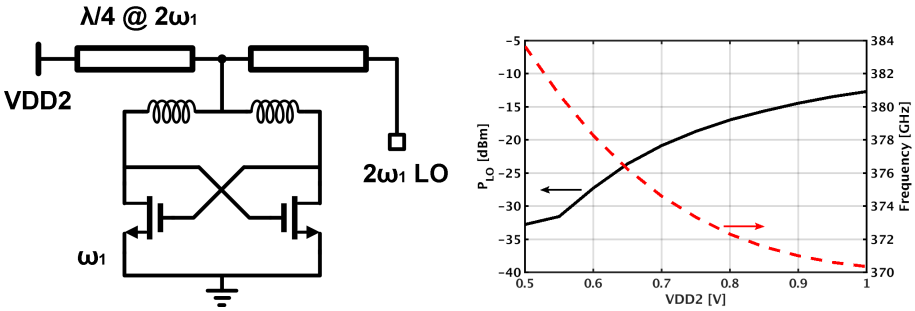


Figure 5.12: Schematic of the push-push VCO to generate the 370GHz LO signal (a) and the frequency and output power when varying VDD2 (b)

5.2.5 210GHz SRO with pre-mixer

The final component of the SRR is the super-regenerative oscillator, of which the start-up behavior is evaluated to determine the amount of THz input power. The schematic of the SRO is given in Figure 5.13: it consists of a cross-coupled VCO and a PMOS envelope detector. The VCO can be quenched by utilizing the NMOS transistor connected between the VCO source and ground as a variable current source. By varying the gate signal Q of the quenching transistor, the bias current through the cross-coupled pair changes and thus enable or disable oscillation start-up of the VCO. The downconverted IF signal at the fundamental frequency of the SRO is injected in the

tank through an NMOS transitor, which is kept small to reduce the additional parasitic capacitance to the tank.

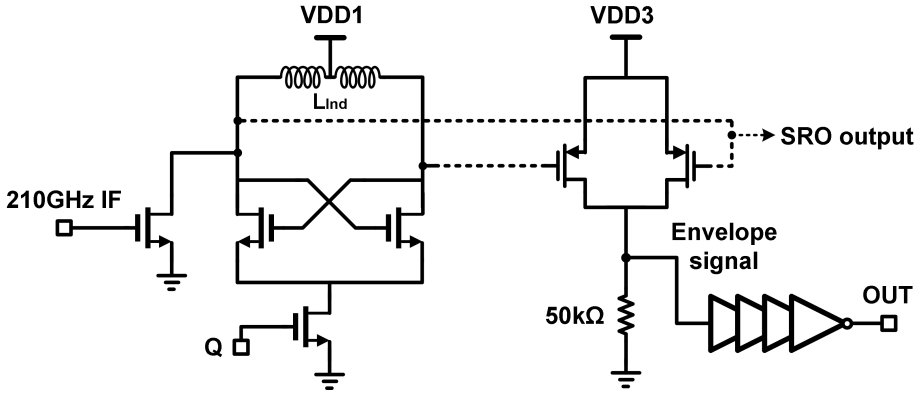


Figure 5.13: Schematic of the 210GHz SRO and square-law envelope detector

To evaluate the start-up behavior, the output nodes of the SRO are connected to a square-law envelope detector which tracks the shape of the SRO's oscillation signal. The envelope detector is implemented by two common-source PMOS transistors with the drains connected together. This results in a current representing the sum of differential output nodes of the SRO. The difference current flows through a $50k\Omega$ on-chip resistor to be converted back to a voltage representing the envelope of the SRO oscillation signal. The large resistance ensures a large enough voltage to be picked up by the inverter chain and brought off-chip, while at the same time acting as a low-pass filter to filter out the 210GHz SRO signal and keep the lower-frequency start-up evolution and quenching pulses. The inverter driver consists of a tapered chain of inverters, capable of driving the 50Ω off-chip input resistance of measurement equipment.

Figure 5.14 shows the transient signals at the nodes of interest in Figure 5.13 during one start-up/damping cycle, with a -20dBm input signal at 584GHz. The quenching signal Q is a sine wave, which provides enough biasing current for start-up at around 0.6V. The oscillation start-up, tracked envelope signal and the converted digital signal through the inverters can easily be distinguished. It is the time of the switching point of the inverter output (when the envelope signal crosses the inverter threshold value) that is used to compare the start-up speed for different THz input powers.

As one is interested in the difference in start-up behavior for different input signal powers, an expression for the oscillation build-up is required. Equation 5.2 describes the exponential increase in tank/SRO output voltage v_{SRO} at start-up, when the losses of the tank R_{loss} are smaller than the negative resistance $R_{neg.res.}$.

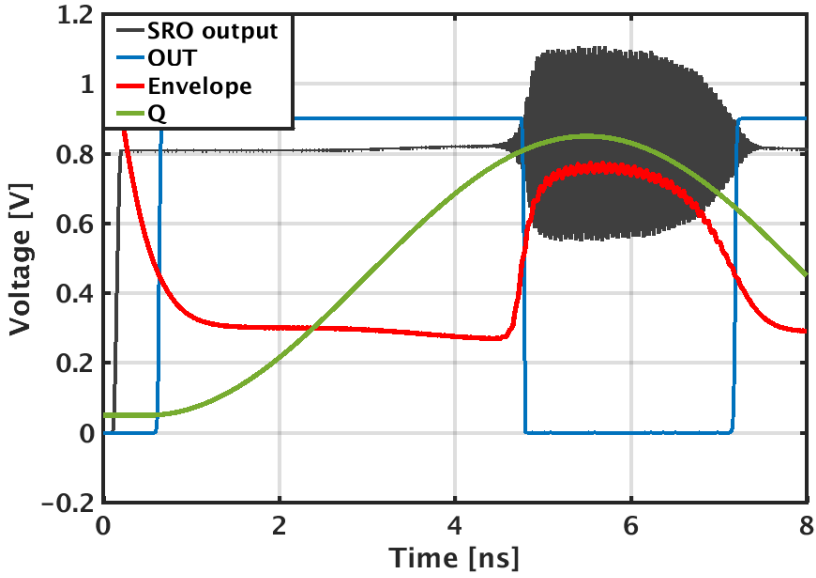


Figure 5.14: Example of the different waveforms at different points (see Figure 5.13) of the SRO and envelope detector chain

$$v_{SRO}(t) = v_{start} \cdot exp\left(\frac{(-R_{neg.res.} - R_{loss}) \cdot t}{2 \cdot L_{ind}}\right) \tag{5.2}$$

$$v_{start} = v_{noise} + v_{injected} \tag{5.3}$$

There are several components that determine the growth of the oscillator signal: the starting value v_{start}, the performance of the cross-coupled transistor pair ($\approx R_{neg.res.}$), the quality of the resonator tank ($\approx R_{loss}, L$). By modifying the parameters, one can hasten or prolong the start-up phase and thus the steepness of the input signal of the envelope detector.

For a larger negative resistance generated by the circuit, the start-up speed of the oscillator increases. $R_{neg.res.}$ depends on the cross-coupled pairs transistor size, biasing and the tank voltage v_{SRO}. For increasing values of the tank voltage, $R_{neg.res.}$ decreases to the point where the generated negative resistance is equal to the tank losses. The tank voltage reaches its saturated level and steady-state oscillation is achieved thanks to this self-limiting of the loop gain. In a quenched SRO, the generated negative resistance is

constantly modified by quenching the cross-coupled pair, which is done by changing the bias current. The quenching signal Q therefore creates periods in time where the negative resistance is sufficient to overcome the tank losses and start oscillation, as well as periods where the generated negative resistance is insufficient and oscillation is dampened. Closely linked to the generated resistance is the total tank loss R_{loss}: higher tank losses slows down the oscillation signal build-up, and for a varying $R_{neg.res.}$ also delay the on-set of start-up. The tank losses are directly dependent on the quality factor of the tank, which illustrates the importance of a high-quality resonator.

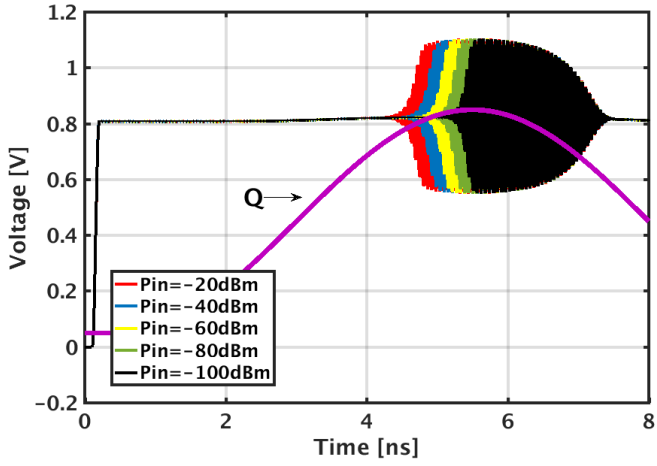
The last remaining parameter, v_{start}, is the only one that depends on the incoming THz signal and thus the one that can be used to influence the start-up speed by applying a different THz input power signal. v_{start} is the starting value of the SRO signal at the fundamental oscillation frequency. In a classic VCO, v_{start} consists of noise, which contains a small component at the target frequency. Thanks to the large loop gain at start-up, this small v_{noise} signal is amplified and fed back until steady-state oscillation is achieved. In the case of an SRR system, v_{start} consists of both the noise-based v_{noise} component and the injected IF signal $v_{injected}$ at the SRO fundamental frequency (Equation 5.3).

If no THz signal is captured by the receiving antenna, there is no IF signal and thus no $v_{injected}$. The oscillator starts up with the same speed and envelope as a classic VCO. However, if a THz signal is present that results in a downconverted IF signal at the fundamental frequency of the SRO, $v_{injected}$ is non-zero and the oscillation build-up process is given an initial head start, which results in the SRO output reaching it's saturated level faster. Incoming THz signals with more power result in more IF signal being injected in the SRO, and in turn results in a larger seed value for the oscillator feedback loop to build up its oscillation signal. By detecting this increase in start-up speed, we can deduce the power of the incoming THz signal and thus implement a THz amplitude/power detector.

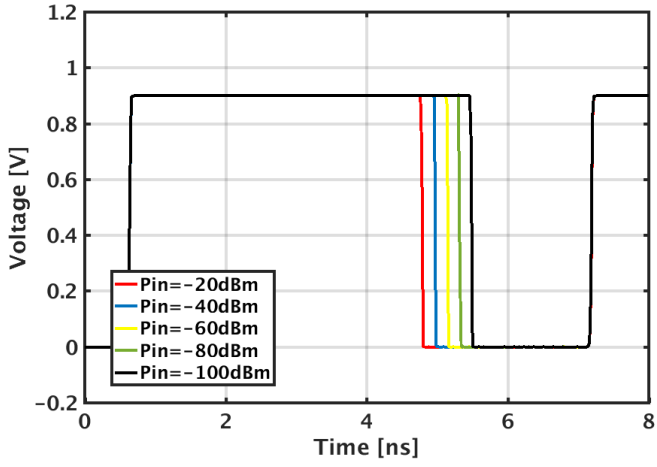
5.2.6 SRR overview

To verify the operation of the SRR, a THz input signal at 584GHz with different input power is applied at the receiver antenna, ranging from -20dBm to -100dBm. For each simulation, the same sinusoidal quenching signal Q is used, with a frequency of 100MHz. Figure 5.15a shows the resulting SRO output signals for varying THz input power, while Figure 5.15b depicts the corresponding digital output of the envelope detector and inverter chain.

Evaluating the difference in start-up speed, one can clearly see that a larger THz input power yields a faster start-up of the SRO signal and in turn a faster transition in the digital output signal of the envelope detector. Once the oscillation signal reaches



(a)



(b)

Figure 5.15: Output signal of the SRO (a) and after the envelope detector and inverters (b) for different THz input powers. The start-up time of the SRO is increased with higher THz input power

saturation, there is no discernible difference in behavior between various input powers. The SRO can now be seen as operating like a VCO which is being injection-locked by the very small IF signal, which is too small to impact the VCO behavior. This confirms that the SRR is sensitive to the incoming THz signal only at the onset of start-up, as discussed in Section 5.2.1. When the quenching signal drops below the necessary value to supply sufficient bias current, the oscillation decays until the oscillator is completely turned off and reset for the next detection cycle.

The envelope detector output is brought off-chip to be analyzed on an oscilloscope to measure the SRO start-up time. This timing measurement could be integrated on-chip by a Time-to-Digital converter (TDC), using the (simple) TDC implementation shown in Figure 5.16. Depending on the start-up time, the output of the envelope detector takes shorter/longer to reach the inverter threshold point. This inverter transition ripples through the inverter delay line and is captured by a series of flip-flops. These take a snapshot of the nodes of the inverter chain after a fixed delay based on the quenching signal (and thus the SRO activation). By converting the position of the ripple in the delay line using a thermometer-to-binary converter, the resulting output is a binary representation of the SRO start-up time and thus the THz input signal strength.

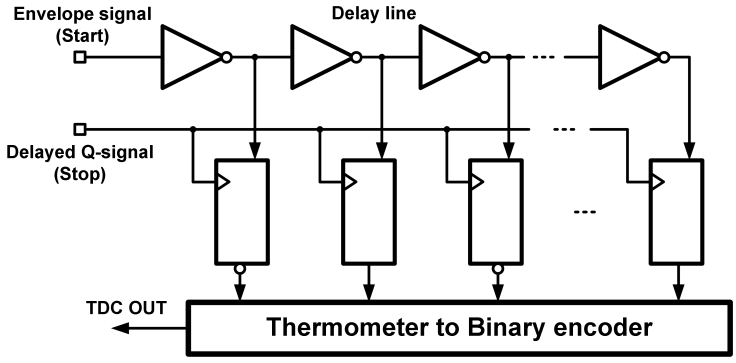
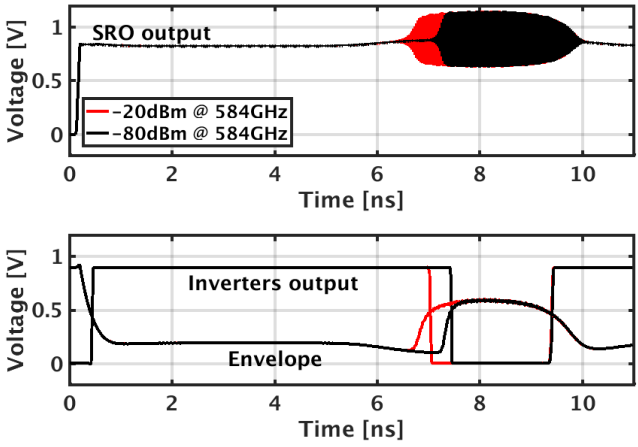


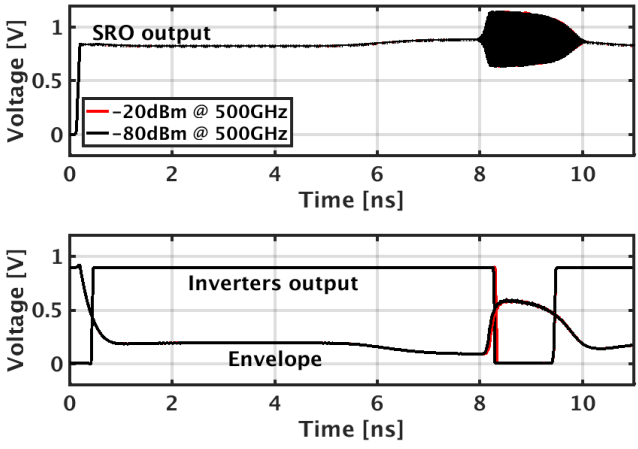
Figure 5.16: Schematic overview of a TDC implementation to measure the difference in SRO start-up time

As the SRR bears similarities to the injection-locked divider, and the operating principle of the SRR is based on the increased value of v_{start} in Equation 5.2, the frequency selectivity of the SRR can be examined. For an injection-locked VCO, the presence of a sufficiently large signal within the locking range of the tank pulls the fundamental oscillation away from it's free-running frequency (Section 5.1.2). In the proposed SRR, the injected signal is too low to pull the SRO frequency. However, it kickstarts the oscillation start-up by providing a larger v_{start} at the SRO's fundamental frequency. If the incoming THz signal would be downconverted to an intermediate frequency that differs greatly from the SRO frequency, the injected signal in the SRO tank would not

start oscillation due to the frequency selectivity of the resonator during start-up. v_{start} would still only consist of the noise value at the SRO frequency, and the start-up speed is not improved.



(a)



(b)

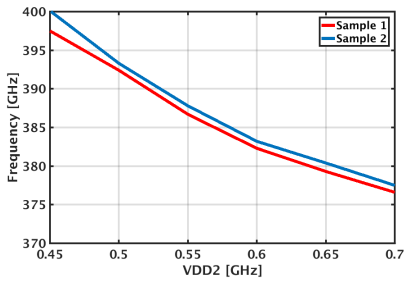
Figure 5.17: SRO waveform (top) and detector output (bottom) for input signals at 584GHz (a) and 500GHz (b)

This is demonstrated in Figure 5.17, where two incoming THz signals at different frequencies are compared. First, Figure 5.17a shows the SRO and SRR outputs when

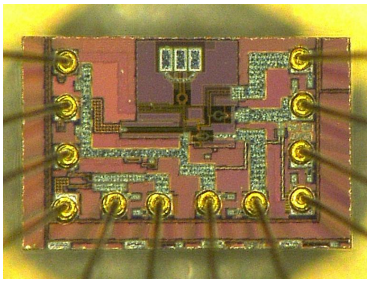
the incoming 584GHz signal downconverts to the SRO frequency. Depending on the input power, the value of v_{start} changes and there is a substantial difference between the falling edges of the SRR digital output. Second, in Figure 5.17b the incoming 500GHz signal downconverts to an IF that falls out of the SRO sensitivity range, and thus does not influence the start-up behavior and timing of the falling edge of the SRR output. By changing the frequency of the LO-VCO, the correct downconverted intermediate frequency can be maintained for various incoming signal frequencies.

5.2.7 SRR measurements

Unfortunately, successful measurements of SRR operation were not possible. The problem existed in the SRO, the central component of the SRR, not starting up. The oscillation frequency of the SRO at 210GHz proved to be too much on the edge of the capabilities of the cross-coupled pair to handle. While a fundamental oscillation frequency of 200GHz has been demonstrated using similar transistors (Section 4.4), the tank losses of the additional SRR components and metal traces that are connected to the oscillator core have probably been underestimated during parasitic extraction. An implementation with probe pads for the input THz signal was also measured, with the hope that a sufficiently large input power would help the SRO to wake up. Alas, the SRO remained silent. It was, however, possible to verify the working of the LO-generating VCO, as the large output power and parasitic radiation enabled the detection of a fraction of the 370GHz LO signal. The tuning range of the LO-VCO goes from 370GHz to 400GHz while keeping a 3dB output power variation, and corresponds to the simulated frequency range of the LO-VCO.



(a)



(b)

Figure 5.18: Tuning range of the LO generator, measured by capturing the parasitic radiation of the VCO (a). Die photo of the SRR (b)

5.3 Schottky Barrier Diode (SBD) detectors

5.3.1 Introduction to SBD

For applications where the detection of incoming THz amplitude or amplitude modulation is sufficient, rectifying devices can be a potential solution to implement THz detectors. This can be done using pn junction diodes, transistors biased in sub-threshold, diode-connected transistors [Kim16] or Schottky Barrier diodes (SBDs). As a result from the rectification of the incoming signals, there is no frequency selectivity. Some frequency selectivity can be achieved by utilizing a narrow-band antenna, but since interfering signals in the THz range are limited and attenuate very strongly over short distances, this is usually not a problem for THz imaging applications.

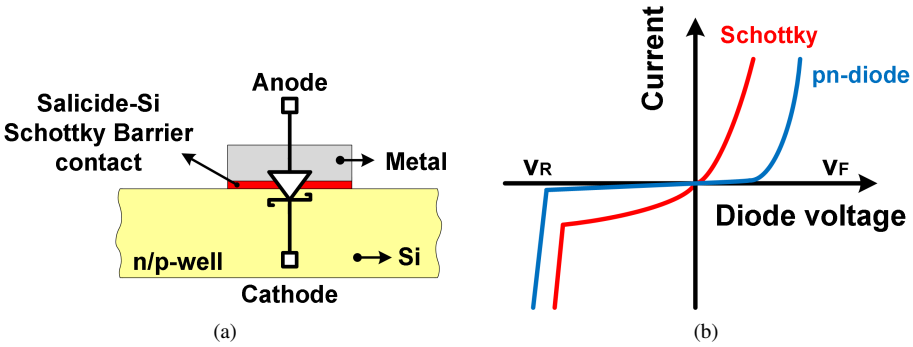


Figure 5.19: SBD symbol and location of the metal-semiconductor junction (a), diode current for a Schottky and pn-diode (b)

SBD diodes differ from regular diodes in their junction: regular pn-junction diodes have a semiconductor-semiconductor junction, while SBD have a metal-semiconductor junction (Figure 5.19a). Their respective I-V curves are shown in Figure 5.19b, where the major difference is that SBD conduct current at much lower forward-biasing voltage V_F than pn-diodes. The downside is that the leakage current in reverse-bias V_R is also larger for SBD compared to pn-diodes. More importantly, SBD can achieve a higher cutoff frequency f_{cutoff} due to the absence of a diffusion capacitance compared to pn-diodes (SBD has no minority-carrier storage, is only a majority-carrier/electron device). Therefore, SBDs implemented in III-V technology have been used for mm-wave and THz applications, and form the core of many high-frequency multipliers and mixers in THz lab measurement equipment [Hes07]. With the advancement of CMOS, Schottky Barrier diode implementations in nanometer CMOS process nodes without requiring special process modifications have been reported [Die17], with cutoff frequencies reaching 2THz in 130nm CMOS [San09]. Using these SBDs, detection of

frequencies up to 9.74THz have been reported in CMOS [Ahm14] which exceeds the estimated cutoff frequency of the device.

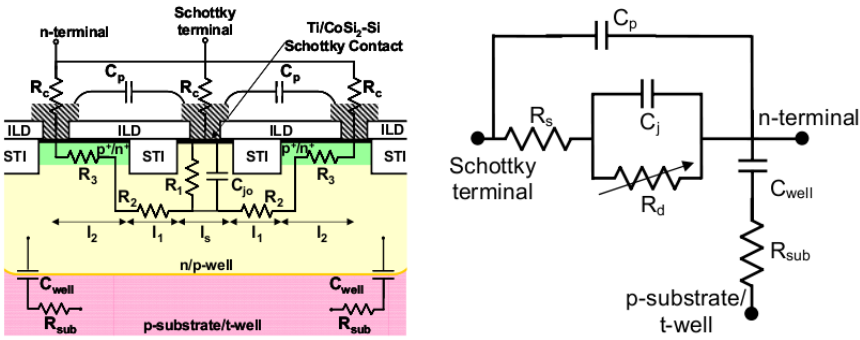


Figure 5.20: CMOS SBD cross-section (a) and equivalent model (b), from [San08]

A cross-section of a CMOS implemented SBD and the corresponding model are given in Figure 5.20. The Schottky barrier contact is realized by depositing a thin transitional metal under the anode terminal (ex. a Ti/CoSi2-Si junction), which overlaps with the silicon. This forms a metal salicide contact or Schottky contact, with the area of the contact determining the size of the SBD. The cathode terminal is then realized by the ohmic contact to the n/p well surrounding the Schottky contact. From the equivalent model, one can divide the SBD into two parts: the first part is the Schottky junction itself, which can be modeled by a variable resistor R_d and junction capacitor C_j. This forms the true SBD. The other components of the model are due to interconnection losses and parasitics: R_s is a series resistance due to the impedance of the n-well material between the Schottky junction under the anode and the cathode, C_p is the parasitic sidewall capacitance between anode and cathode terminals and C_{well}/R_{sub} are due to substrate losses.

The high-frequency performance of a SBD is limited by the cutoff frequency f_{cutoff}, due to the RC filter formed by R_s and C_j, and can be defined as follows:

$$f_{cutoff} = \frac{1}{2\pi \cdot R_s \cdot C_0} \tag{5.4}$$

$$C_0 = C_j + C_p \tag{5.5}$$

To maximize f_{cutoff}, both R_s and C_0 should be minimized. C_0 depends on the sidewall capacitance C_p and the diode junction capacitance C_j. This junction capacitance is

derived from the area of the Schottky contact, so a minimum diffusion contact area should be utilized. The series resistance R_s can be minimized by reducing the spacing between anode and cathode. Unfortunately, this cannot be minimized too much before the parasitic sidewall capacitance of the higher interconnecting metals start increasing too much and cancel any gains made by reducing the well resistance.

5.3.2 Design of a THz SBD receiver circuit in 28nm CMOS

For the implementation in 28nm, a diode detector setup similar to [Han13b] is used where an antenna is directly connected to a number of Schottky diodes in parallel. The goal is to use the SBD as a rectifier of the THz signal, and be able to measure the received power. A schematic of the THz SBD system is given in Figure 5.21. The on-chip antenna captures the radiated THz signal and feed it to the SBD, which rectifies the signal to a baseband signal. The SBD is forward-biased by means of a large off-chip resistor R_{bias}, connected through a DC feeding point on the antenna.

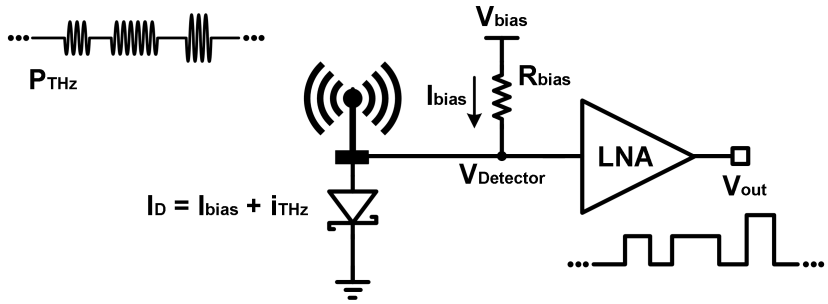


Figure 5.21: read-out circuitry

$$i_D = f(v_D) = I_S \cdot \left[exp\left(\frac{qv_D}{nk_BT}\right) - 1 \right] + G_{term} \cdot V_{term} \tag{5.6}$$

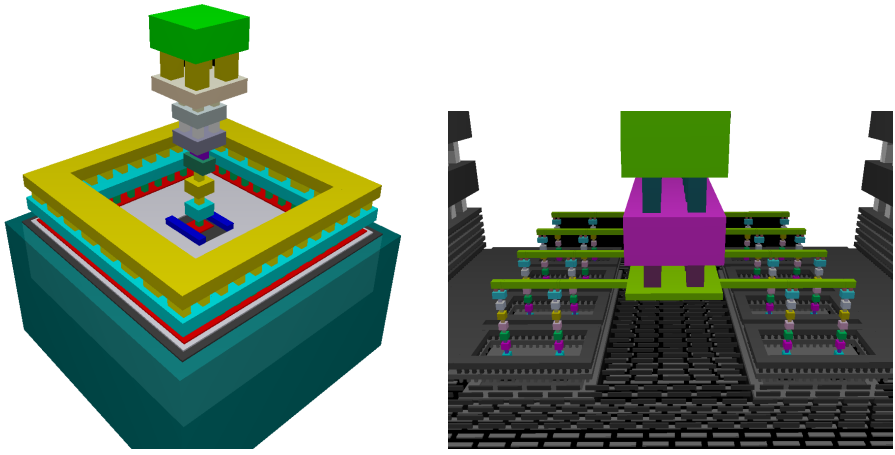
$$v_D = V_{bias} + A_{RF} \cdot cos(t \cdot 2\pi f_{RF}) \tag{5.7}$$

The current through the SBD depends non-linearly on the diode voltage v_D. This non-linear relationship is given in Equation 5.6, with I_S the diode reverse saturation current, q the electron charge, v_D the diode voltage, n the diode ideality factor (approximately 1), k_B the Boltzmann constant and T the operation temperature. The last term ($G_{term} \cdot V_{term}$) gives the leakage current between the two diode terminals, which results in a constant DC offset.

As the diode voltage is comprised of a DC bias voltage (V_{bias}) and a THz signal (Equation 5.7), the diode current has a DC current consisting of a component I_{bias} due to V_{bias} and a current component i_{THz} due to the rectification of the THz signal to baseband. This current flows throught the diode junction resistor R_D and results in a DC voltage which changes depending on the signal power of the incoming THz signal. The difference in voltage (Δv) due to the rectification of the THz signal is given in Equation 5.8. It depends on the square of the incoming signal (hence "square-law detector").

$$\Delta v \approx \frac{A_{RF}^2 \cdot q}{4 \cdot n k_B T} \tag{5.8}$$

By modulating the amplitude of the incoming THz signal and measuring the $V_{Detector}$ voltage, a THz power detector system is achieved. The frequency of the OOK modulation or chopping frequency upconverts the output signal of the detector to the modulation frequency instead of DC, reducing the influence of flicker noise on the receiver. An LNA is used to capture and amplify $V_{Detector}$. The noise of the LNA should be lower than the flicker noise of the diode and have a sufficiently high bandwidth to allow the increase of modulation frequency to lower the diode flicker noise.



(a) (b)

Figure 5.22: 3D layout of a single SBD (a) and a 8x2 SBD implementation (b)

The SBD unit cell is shown in Figure 5.22. To maximize the cutoff frequency of the diode, a minimal Schottky contact area is implemented to minimize the junction capacitance C_j. Several of these SBD unit cells can be combined in parallel to increase

the total diode size. Figure 5.22b shows 8x2 SBD unit cells combined to create a SBD test structure with 16 parallel SBD cells.

5.3.3 Bowtie antenna design, from 500GHz till 30THz

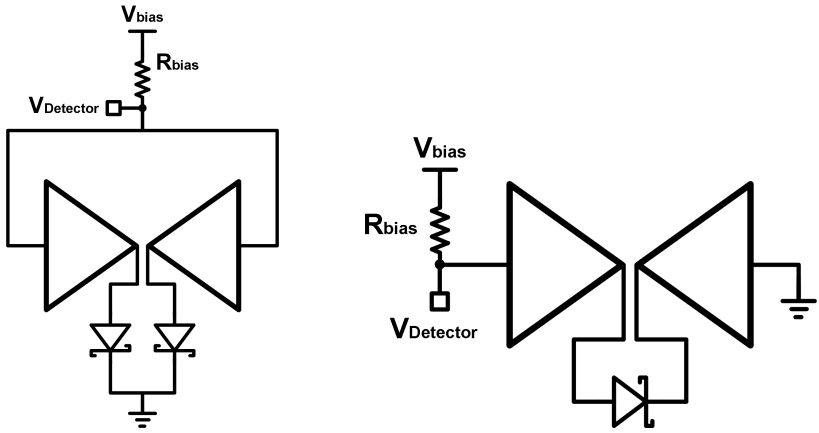
Design of on-chip bowtie antennas for THz SBD detectors

For the design of the THz SBD detector, a broadband on-chip antenna is preferred. The broadband characteristic would be a useful feature, as this allows the SBD detector to be used over a large frequency range as the diode is not very frequency selective. Other unwanted high-frequency signals could thus be picked up and rectified, resulting in a DC offset voltage. Since the wanted THz signal is modulated with a known frequency, this DC offset due to unwanted signals can be filtered out together with the diode forward bias current. In addition, due to the high FSPL attenuation at THz, the presence of interfering signals in the same frequency band is limited.

First discussed in a patent application in 1898 by O. Lodge [Lod89] [Sch04], biconical antennas are known for their broadband characteristics. They consist of two conical conductive parts which come together at the positive and negative antenna terminal, which is the signal feed point. An on-chip variant can be implemented by two metal triangles, resembling a butterfly or bowtie. This antenna is sometimes also referred to as a triagular dipole, as it shares similar radiation pattern properties with the classic dipole antenna. At the point where the two triangles meet, SBDs can be placed in parallel or in series with the two bowtie antenna halves to rectify the incoming THz signal as illustrated in Figure 5.23.

The dipole antenna is a resonant antenna, as it can only radiate efficiently at frequencies where its length is a multiple of the half wavelength of the target frequency. The radiating performance of the classic dipole antenna is therefore specified by the length of the antenna, which does not meet the half wavelength requirements for all frequencies. The bowtie antenna, however, is a traveling-wave antenna: radiation is achieved through a traveling wave on a guiding structure (similar to a transmission line), in this case the bowtie triangles. For an infinite cone length, the bowtie antenna would operate efficiently at all frequencies, and the characteristic impedance would only depend on the angle of the antenna cones. For practical reasons, the bowtie antenna has a finite length, which should be long enough to accommodate the longest wavelength of the target frequency band. The simulated electric field in a multiple-λ bowtie antenna is shown in Figure D.2, where the traveling wave is clearly visible.

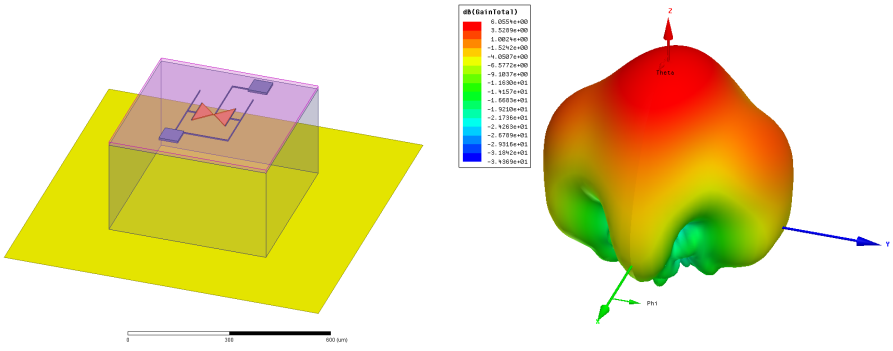
The angle of the bowtie antenna cones was chosen to be 45°, as this was the only angle compliant with the design rules of the 28nm CMOS process. Other cone angles could be realized by implementing a stair-like polygon consisting of 90°angles, but



(a) (b)

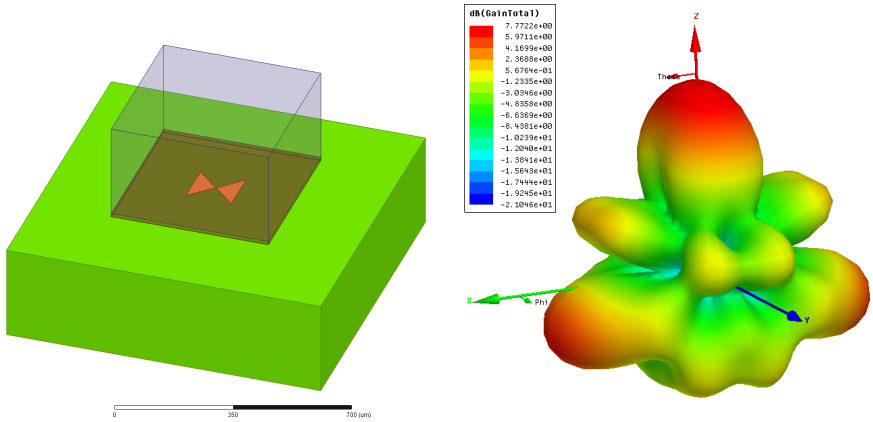
Figure 5.23: Schematic of SBD connected to a bowtie antenna in parallel (a) and series (b) between the bowtie cones

this was not used in this design. As the impact of cone length has a limited impact on the radiation performance, the packaging of the die with on-chip bowtie antenna has a major influence on the radiation pattern and efficiency. Three packaging solutions are evaluated for the bowtie antenna: bondwires and PCB reflector (Figure 5.24), flipchip without reflector (Figure 5.25) and flipchip with a reflector at the bottom of the mounting PCB (Figure 5.26).



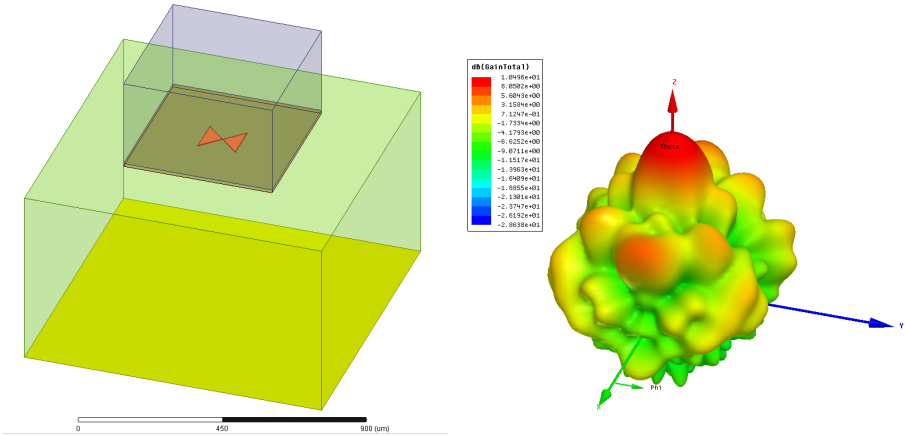
(a) (b)

Figure 5.24: Model (a) and radiation pattern (b) of a wire-bonded on-chip bowtie antenna with PCB reflector at 800GHz



(a) (b)

Figure 5.25: Flipped bowtie antenna model (a) and radiation at 500GHz (b). Simulated directivity pattern is included in Figure D.3



(a) (b)

Figure 5.26: Flipped bowtie antenna with PCB reflector model (a) and radiation at 900GHz (b). Simulated directivity pattern is included in Figure D.3

As the SBD is to be used as a broadband detector, different antennas and antenna packaging solutions at frequencies ranging from 500GHz to 1THz have been simulated, of which some are given in Table 5.1. From these results, one can conclude that for similar bowtie antennas, the performance can drastically change for different frequencies and packages. While the packages with reflectors achieve a higher directivity, their radiation efficiency η_{rad} is lower as part of the THz radiation has to travel twice through the lossy silicon substrate. The flipchip packages have an additional degree of freedom in the form of the mounting PCB height, which depending on the thickness adds constructively or destructively to the upwards radiation. This is especially the case when a metal reflector is used at the bottom of the PCB, similar to the flipchip dipole in Section 5.2.2. Figure D.4 shows the radiation pattern of the same bowtie antenna at 800GHz in a flipchip package and a bondwire and PCB reflector package, illustrating the importance of selecting the right packaging method for the target frequency. An example of the simulated antenna impedance is included in Figure D.5 for a bowtie antenna with a 50μm arm length and PCB reflector.

Table 5.1: Antenna properties of varying bowtie antenna packaging solutions

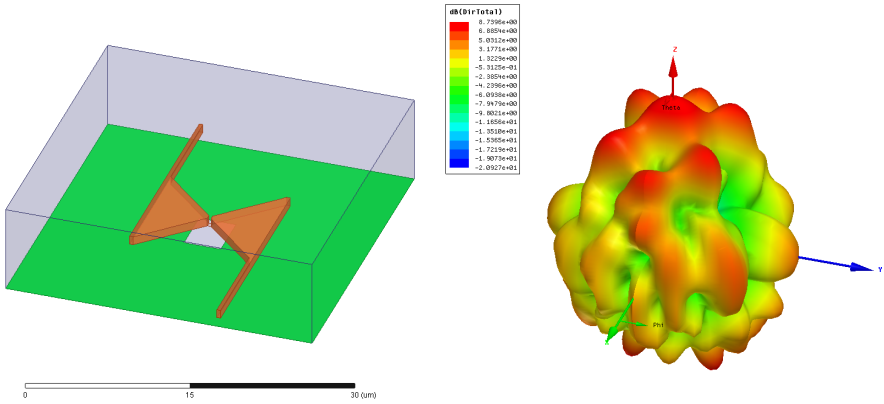
Freq. [GHz]	Length	Package	Reflector	G_{ant} [dB]	D_{ant} [dB]	η_{rad} [%]
500	40-70	Flipchip	No	7.8	9.8	63
600	50	Flipchip	Yes	7.8	12.3	36
800	70	Bondwire	Yes	6	10.8	33
800	70	Flipchip	No	-3.7	-6.7	51
900	60	Flipchip	Yes	10.5	14.5	40
900	50	Bondwire	Yes	4.2	12.6	14
1000	40	Flipchip	Yes	7.6	12.2	33

Bowtie antenna design for a 33THz SBD thermal imager

To push the frequency of the detector above 1THz, measurement equipment would be needed to generate this frequency. Due to a lack of measurement equipmentm, [Ahm14] uses a dimmed fluorescent lamp to generate a 9.74THz signal measuring an SBD detector at this frequency. Going higher in frequency, in the long-wavelength IR (LWIR) spectrum, commercial Fabry-Perot QCLs are available with a wavelength of $9.15-10\mu$m (30-32.7THz). This frequency range is interesting, as infrared thermography or "thermal imaging" is done in this band of wavelengths ($9-14\mu$m). The human body for example radiates mainly at wavelengths of 10μm. If a detector could be made in this frequency band, a low-cost CMOS thermal imager can be realized. A single SBD cell is used for the design of the 30THz detector. Even if this is higher than the cutoff

frequency of the diode, a strong enough input signal could still yield enough output signal to be detected.

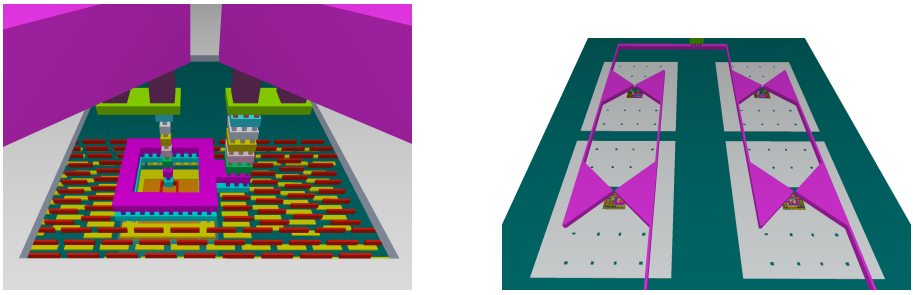
To capture this 30THz signal, an on-chip bowtie antenna is implemented in the M8 layer. As the wavelength at this frequency is close to 5µm, the 12.5µm length equals a $\approx 2.5\lambda$ bowtie antenna. However, simulating a 12.5µm bowtie at 30THz on top of a 300µm thick substrate requires an enormous amount of computational power and time. As this was not feasible, a metal reflector is placed under the bowtie to shield the antenna from the substrate, and thus drastically reduce the simulation model. Additionally, a correct placement of the reflector can increase the radiation pattern of the antenna by adding the reflected radiation to the top-side radiation through constructive interference. Due to the high frequency and small wavelength, only 1.25µm spacing is required between the bowtie and the metal reflector plane to result in a $\lambda/4$ spacing and constructive interference. This can be achieved by creating a large metal plane in a lower metal (M6) of the 28nm CMOS process. The 3D simulation model and radiation pattern are given in Figure 5.27. The simulated directivity is 8.74dB with a high radiation efficiency of 91.4%.



(a) (b)

Figure 5.27: Simulation model (a) and radiation pattern (directivity) (b) of an on-chip 30THz bowtie antenna

Since the terminals of the bowtie in the top metal layer should be connected to the bottom metal layers to reach the SBD, an opening is created in the reflector (Figure 5.28a). The SBD is biased through feed lines connecting to the sides of the bowtie antenna, which yielded a 2dB increase in directivity compared to feed lines arriving in the center of the bowtie as was done for the other antenna designs. Due to the small size of the antenna, a 2x2 bowtie antenna array can be implemented while remaining the same size of a bond pad (Figure 5.28b).

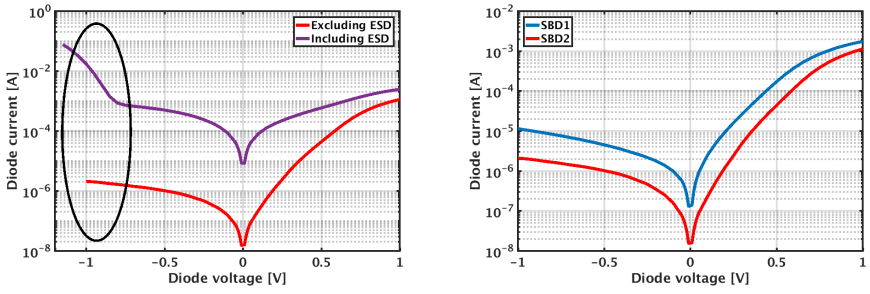


(a) (b)

Figure 5.28: Close-up of the bowtie-SBD connection through the opening in the M6 reflector plane (a) and 2x2 array of 30THz bowtie antennas (b)

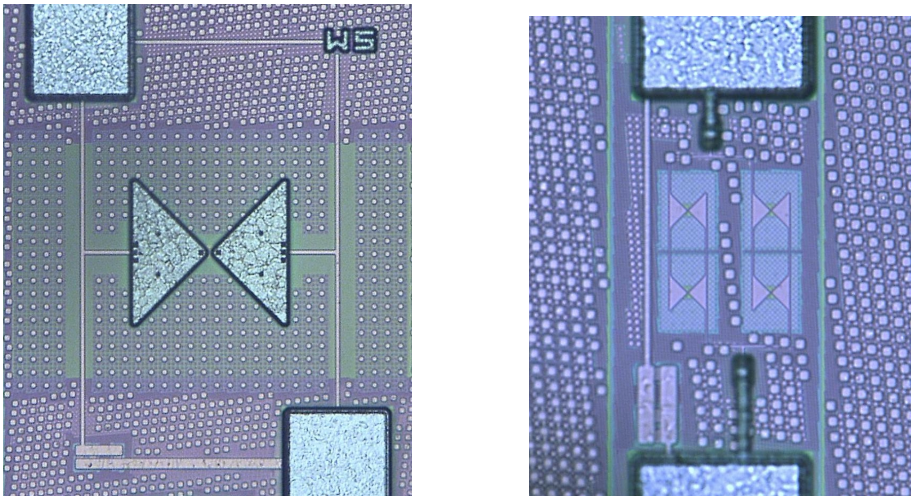
5.3.4 SBD measurements in 28nm CMOS

DC measurements of a diode test structure containing 32 SBD unit cells have been done to create I-V graphs of the diodes and attempt to characterize the fabricated SBD. The I-V plots are shown in Figure 5.29. The initial measurements indicated that the ESD-protection diodes between supply and ground had a negative impact on the I-V curve. By cutting the metal trace to the ESD cells with a high-power laser, the ESD diodes were removed. The resulting I-V curve has the characteristics of SBD behavior, albeit with a larger than expected leakage current when reverse-biased and lower current in forward bias. Due to the small dimensions of the SBD cells, small process variations have caused noticeable differences between chips, as illustrated in Figure 5.29b. Further measurements and study are required for the modeling of the SBD diodes, as well as measuring their THz rectification capabilities (Figure 5.30).



(a) (b)

Figure 5.29: Measured SBD test structure current with (a) and without (b) ESD diodes connected



(a) (b)

Figure 5.30: Die photo of (a) on-chip bowtie antenna and SBD detector and (b) 2x2 30THz bowtie antenna array

5.4 Conclusion

In this chapter, an overview of several receiver topologies for THz detection has been given. A THz SRR with dual-gate pre-mixer has been designed to receive a 580GHz signal. The large LO power required to drive the dual-gate mixer is provided by an on-chip LO generator, implemented by a push-push VCO. For the on-chip antenna, a flipchip dipole is used to improve the performance of the antenna compared to a wire-bonded dipole antenna. Second, diode-based detectors utilizing Schottky barrier diodes with broadband on-chip bowtie antennas have been designed to detect signals ranging from 500Ghz to 1THz, with a miniature version designed to detect 30THz. The simulated bowtie antennas can be utilized in both bond-wire and flipchip configurations. Unfortunately, these results could not be verified with measurements.

Chapter 6

Conclusions and future work

6.1 Overview of the presented work

The THz spectrum remained practically unattainable for both electric and optical devices due to its tremendously high frequency. This lack of available devices has resulted in very limited commercially available THz applications, referred to as the infamous 'THz gap'. Bridging this THz gap would enable a wide range of possible game-changing applications, as the properties of the THz spectrum prove to be a blend of the best characteristics of both microwave and optical. Transparency in most materials, non-ionizing radiation, large bandwidth for Tbps communication links or high-precision radar, sub-mm spatial resolution, spectroscopic capabilities, ...

In the past decade, the scaling of CMOS has increased the operation frequency of integrated circuits, with f_{max} reaching 300+GHz in deep-scale nanometer CMOS nodes. While this is not sufficient to implement fundamental signal generators and amplifiers, the usage of harmonics of sub-f_{max} circuits to generate above-f_{max} signals enables the realization of THz integrated circuits in CMOS. The increase in frequency also allows for the implementation of on-chip antennas and couplers together with the sources and receivers, resulting in fully integrated, compact THz systems.

This work focuses on the design of low-cost, compact THz circuits with integrated antenna solutions and their potential applications. The realization of THz circuits in CMOS would enable very cheap, mass producible chips which will find their way in a cornucopia of applications on both consumer and industrial level. The frequency limitations of CMOS have been overcome by utilizing harmonics and several THz transmitters have been realized in cutting-edge CMOS process nodes (40nm, 28nm), reaching state-of-the-art operation frequencies from 0.54THz up till 0.61THz.

The design of several THz receiver topologies is also presented, including injection-locked dividers, super-regenerative receivers at 580GHz and Schottky barrier diode detectors with on-chip bowtie antennas for broadband THz detection (500GHz-1THz). The absence of gain at THz frequency in CMOS limits the receiver performance and

design flexibility, as well as requiring large incoming THz power or LO generation at mm-wave. Accurate, efficient THz receivers remain difficult to implement and present an important roadblock for the breakthrough of THz into commercially available sensor systems.

The fabricated chips of this work are used in THz imaging systems, and successfully demonstrated a variety of cases and applications where THz radiation can have a significant, positive impact. The realized THz signal generators are equipped with on-chip antennas and take up minimal silicon area, proving the feasibility of low-cost, high-density and easily packageable THz radiator arrays.

6.2 Research contributions

An overview of the major research contributions of this work towards the design of THz electronics in CMOS and the exploration of issues, solutions and applications is given;

- In-depth analysis of the impact of both transistor and passives layout on the high-frequency performance of integrated circuits is presented. Guidelines and optimal layout strategies for pushing the f_{max} of CMOS transistors to the edge of the technology's capabilities are given. The high-frequency behavior of passives is modeled and discussed. With decreasing CMOS node size, the design rules and metal densities are becoming more strict and dense. While other work on dummy metals has been reported up to 60GHz, this work demonstrates their impact at THz frequency as well as insights in how to minimize their influence.
- Investigation into and comparison of several on-chip antennas and IO transmission methods to be used as part of THz transmitters and receivers. Besides antenna types, the impact of different packaging solutions (flipchip, metal reflectors) and the potential of 3D-printed resonator structures and lenses is evaluated, discussed and implemented.
- Design and implementation of a 0.54THz signal source with 22GHz bandwidth in 40nm bulk CMOS. The transmitter has been measured using both an on-wafer probe and an integrated on-chip dipole antenna. Measurements and simulation results fit very well, validating the used RF transistor model and design methodology. The measured tuning range, 3dB bandwidth and total die area are state-of-the-art, and this chip has the highest single-cell radiated power above 400GHz without utilizing lenses or other package improvements.
- The feasibility of THz CMOS transmitters for imaging applications is demonstrated by utilizing the fabricated 0.54THz signal source in a variety

of imaging applications. Dielectric contrast imaging of different material types has been investigated. The high THz attenuation at 0.54THz due to the absorption peak of water molecules is exploited to create a contactless, non-destructuve humidity detector which would enable sensor applications in both medical as agricultural industry.

- A 0.57THz transmitter with folded dipole antenna and a 0.61THz transmitter with collinear broadside dipole array were designed and fabricated in 28nm bulk CMOS. To the authors knowledge, this is the first 200GHz+ transmitter implemented in the 28nm CMOS node. The implemented transmitters have the highest reported operating frequency and tuning range above 400GHz CMOS signal generators. The core and total die area are among the most compact THz transmitters, including the on-chip antenna. The designs are fully compliant with the strict and limiting 28nm CMOS design rules, including dummy metal density.
- Demonstrated the benefits of THz imaging in a real-life industrial application for the non-destructive, contactless testing and verification of surgical needles. The 28nm CMOS THz transmitters are used as CW signal generator. Due to the high operation frequency, a sub-mm spatial resolution can be achieved, which is necessary to accurately detect any bending of the needles while they remain in their package.
- An investigation and comparison between receiver circuits is done, with several designs to receive and detect 500+GHz signals using SRR and SBD detectors. The design of an integrated 30THz SBD detector for thermal imaging is discussed, as well as the on-chip 30THz bowtie antenna. The fabricated receivers are the first THz detectors using SBD in 28nm CMOS, and require additional measurements.

Above all, this work is an initial research effort towards the fabrication of THz CMOS integrated circuits, combined with the on-chip integration of antennas and exploration of possible THz applications (THz imaging in particular). This work discusses many of the issues at the boundaries of these fields, and presents solutions and examples of successful THz electronics in CMOS. The following sections will discuss future work for the three areas that have been investigated in this work: THz circuits, THz antennas and THz applications.

6.3 Future work: increasing the output power and frequency of CMOS circuits

One of the main achievements of this work is the demonstration of signal generators above 500GHz in deep-scale nanometer CMOS technology. The THz imaging

experiments validate that the CMOS sources, even with their rather limited output power, can be used effectively for a variety of valuable THz applications. To further improve the performance of these THz imagers, there are two research paths that should be explored in parallel: increasing the output power and pushing the operating frequency higher.

The increase in output power can be done on an oscillator level by changing the harmonic oscillator topology, utilizing harmonic extraction of heavily distorted oscillators and improving the matching requirements at different fundamental and harmonic frequencies. However, the largest improvement will come though combining different oscillator cells together. This evolution towards coupled CMOS oscillators is already underway around 300GHz: lowering the fundamental frequency to mm-wave frequency allows the usage of more complex system techniques, more design headroom and better transistor models and power/phase noise/oscillation generation performance. Translating these design methods to locking and combining several 500GHz+ oscillator cores will prove to be an interesting research challenge and essential step in increasing the total output power in the THz spectrum.

Another important path to pursue is the increase of oscillation frequency of the signal generator cell. With the current outlook on the f_{max} evolution for nanometer CMOS and FinFET nodes, it seems that pushing the fundamental frequency above 300GHz will prove to be very challenging in the near future. Higher-order harmonics could be used to increase the generated frequency beyond the 0.61THz presented in this work, at the cost of lower DC-to-THz power efficiency on account of the higher harmonic number. Consequently, the ideal THz signal generator in CMOS will feature both a high harmonic number and a large array of coupled oscillator cores to provide the necessary output power.

On the topic of THz receivers, the path forwards remains open with possibility. While several successful power/amplitude detectors have been reported at frequencies up to 1THz, frequency selectivity and most importantly phase recovery remain absent. Receivers that can preserve phase could add a huge amount of extra information useful in imaging and radar applications, such as the estimation of relief and depth [Sta11]. Due to the low transmitter output power and high FSPL, receivers with high sensitivity will be required when increasing the distance between transmitter and receiver. For frequencies above 1THz, fast-switching SBD or cold-mixing transistors will remain the most prominent candidates for THz detection in the short term.

Finally, while newer process technology can boast faster intrinsic devices, the actual design and implementation of THz circuits with these devices no longer always result in better performance [Sch15]. Besides the speed of the intrinsic transistor, the metallization options, accuracy and reliability of transistor models have a major impact on the designers ability to implement, simulate, predict and optimize a circuit that will match well with measurements. In addition, the ever tighter restrictions,

design rules and process requirements in deep-scale CMOS, such as metal density, single-orientation transistors and reduced supply voltage, further reduce the design freedoms and usable design techniques. One of the defining aspects of future THz electronics efforts will be the selection of the optimal process technology and frequency for the target application.

6.4 Future work: more efficient antennas and IO

Most of the design presented in this work are equipped with on-chip antennas to radiate and capture THz signals. Several antenna types and packaging solutions have been discussed. The mentioned antennas have been relatively simple designs, as the main focus of this work is THz circuit design. Therefore, future work towards the improvement of the on-chip antennas could benefit the overal performance of the THz transmitters and receivers.

Detailed and focused research efforts into CMOS compatible THz antennas would yield more compact, more directive and higher efficiency antennas that can be integrated on-chip. An important aspect of this THz antenna research should be the co-design between antenna and circuit, as they depend on each other in both on-chip integration and towards the target specifications.

In addition to the design of the on-chip antenna, further investigation is required in selecting and modifying the packaging and mounting of the THz circuits, as they can have a large influence on the radiation capabilities of the TX/RX. The usage of silicon lenses and flipchip mounting can dramatically improve the radiation pattern of the antenna. While lenses pose a significant additional cost that may not be compatible with CMOS' low-cost appeal, flipchip should prove to be a cost-efficient improvement of the radiation performance. The advancements in high-resolution 3D printing will only further expand the design freedom to improve THz radiation, including the design of costum dielectric lensen, on-wafer printing of SIW, horn antennas and couplers.

Thirdly, there is also the possibility of handling the THz radiation off-chip where more area and design flexibility is present. The flipchip mounting method has been proven to extend up tp 500GHz [Sin17], meaning that THz signals could be transported over PCB transmission lines to the target receiver chip (for chip-to-chip communication). More interestingly, this could also open the way to THz off-chip antennas or dielectric couplers. These off-chip antennas can be larger in size and more complex than their on-chip counterparts, improving the radiation performance and efficiency. This also facilitates the stand-alone testing and characterization of the THz antennas without the need of a co-integrated THz chip. Off-chip coupling structures could also facilitate the transition of THz signals into metal or dielectric waveguides for short-range, wireline communication links, relaxing possible alignment issues.

6.5 Future work: faster, better, more ingenious applications

Even with the limited output power and antenna directivity available from the implemented THz signal generators, this work demonstrated several THz imaging application cases that illustrate the potential of the THz spectrum.

Tbps communication links over relatively short distances will be enabled by the large bandwidths available in the THz spectrum, but will require extensive research on both circuits and directive and efficient wireless/wireline links. However, lower-frequency bands will first be exploited [Boe14] [Kat16]: only when the whole mm-wave spectrum is congested, will the available bandwidth in the THz spectrum warrant the increased complexity of THz circuit design for communication links. Besides high-speed communication, there is a wide range of applications that can benefit from the unique properties of THz radiation, of which THz imaging is destined to result in near-future commercialization. Further exploration of the potential benefits of a THz humidity detector could lead to applications in a variety of sectors: water detectors in bottling facilities, leakage detection, humidity sensors for agriculture and food processing industry, sensor tags for plants in greenhouses, ...

The spectroscopic properties of the THz spectrum could also be utilized for the fabrication of very compact, accurate and low-cost gas sensors. The contactless scanning of surfaces and the non-destructive thickness measurements of materials and coatings, currently done by cumbersome, expensive laser-based or X-ray systems, could be replaced by a high-density array of THz sensor at a fraction of the cost. Medical imaging for cancer and tumor detection using the non-ionizing THz radiation is producing hopeful results, but the long clinical trials, high compliance costs and heavy regulated sector will delay the near-future commercialization of THz technology in the healthcare sector and could prove an insurmountable roadblock for some research groups.

While we can sum up a large number of possible THz applications, the truth is that the advances of THz technology and the improvements of transmitter and receiver systems in CMOS will fuel the creation and development of applications and user cases that can not even be envisioned today. It is therefore important for research into possible THz applications to always keep the capabilities and developments of current state-of-the-art THz circuits and antennas in mind.

6.6 Conclusion and closing remarks

There is still a lot of possible improvement to be made in all domains that comprise THz electronics. Each domain has its own required skill set, challenges and focus points (Figure 6.1), and each would merit several doctorates of research. However, it is important to note that these three domains overlap with each other when it comes to THz: it is difficult to independently design the different aspects of the THz system and maintain an optimal result when integrating the different parts together.

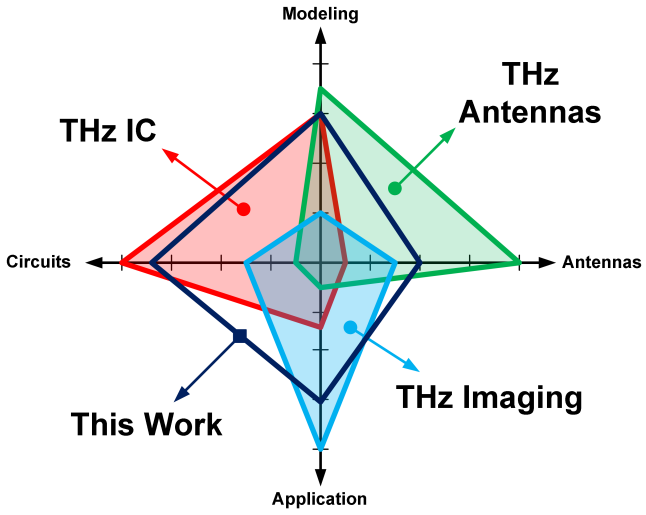


Figure 6.1: Radar chart indicating the required skill set for the different aspects of THz design, and the corresponding breadth of the research presented in this work

It is by looking at the needs, difficulties and challenges of the other THz domains that truly innovative and valuable solutions can be accomplished. There is no benefit in building an application that requires phase information if phase recovery has not been achieved yet in the IC level. At the same time, the large added value of phase recovery to an imaging application might be the catalyst to research a new transceiver topology. The choice of substrate, thickness and metallization option impact both the antenna and IC designer. Co-design between the different THz domain is not only necessary because of integration, but can also alleviate short-comings in one domain by solving it in another: low-power signal generators can be equipped with high-gain antennas, while compact, low-directivity on-chip antennas can be driven by several coupled oscillators or used in applications where omnidirectional radiators are preferred.

In this work, we came into contact with all aspects of THz electronics: the research results on integrated THz circuits in CMOS, as well as on-chip antennas and THz

applications were presented. The main focus of this work remained on the design and implementation of integrated circuits, both from a personal interest and integrated circuits being the first and last hardware components in any communication or imaging system.

The advancement of technology only recently allowed CMOS to access the THz frequency spectrum, meaning that many more fascinating discoveries and circuits will be made in the near future. THz CMOS is located on the intersection of different research domains: the edge of circuits' high-frequency ability, challenging antenna and IO environments due to high attenuation and FSPL, and an affluence of potential applications that utilize the unique characteristics of THz radiation. It is this uncharted territory, this multi-faceted challenge and broad freedom for exploration and innovation that makes THz research so alluring and rewarding. It is the potential for creative research and promising applications that will guarantee that future work in THz electronics will continue to flourish, continue to amaze and provide fantastic opportunities to those who take on its tremendously high-frequency challenge.

Appendix A

Additions to Chapter 2: Sub-mm wave CMOS components

A.1 Transistor gate interconnect for f_t and f_{max}

In Section 2.2.2, the importance of using multiple narrow fingers with double gate contacts was shown when transistors are to be pushed to the limit of their high-frequency potential. In this section, a closer look will be taken at the contribution of the interconnecting network of metals that combines the different narrow fingers of a multi-finger RF transistor. Consider the three gate routing strategies for a $16x1\mu m$ transistor in a 28nm CMOS process shown in Figure A.1. The first approach (Layout A) uses a single gate contact, which are all connected on one side of the transistor. The second approach (Layout B) takes the design of Layout A and connects all the gates together at the opposite side as well, without a direct connection to the gate terminal. While both sides of the gates are shunted together, their voltage is not the same. The final routing solution (Layout C) shunts both gate sides together and connects them through an additional metal trace, so both sides of the gate are at the same gate voltage.

The resulting f_t and f_{max} are simulated and shown in respectively Figure A.1a and Figure A.1b. Looking at f_t, it is clear that the additional metal interconnect traces of Layout B and C result in a lower f_t. From Equation 2.3, we know that the gate resistance R_g does not influence the f_t behavior, and thus we can conclude that this drop in f_t is due to the additional gate capacitance caused by the extra interconnecting metals.

However, when evaluating the f_{max}, which does include R_g (Equation 2.6), the benefit of the double gate contacts of Layout C is clearly visible. Even though the parasitic gate capacitance is larger, the severe reduction of the dominant R_g (by a factor of 4) yields a much higher f_{max} figure compared to Layout A. An important requirement for this reduction is that both sides of the gates should have the same voltage, which can be achieved by the extra metal connections on the side of the transistor. Excluding these extra connections and leaving one of the gate sides as a floating node (Layout B)

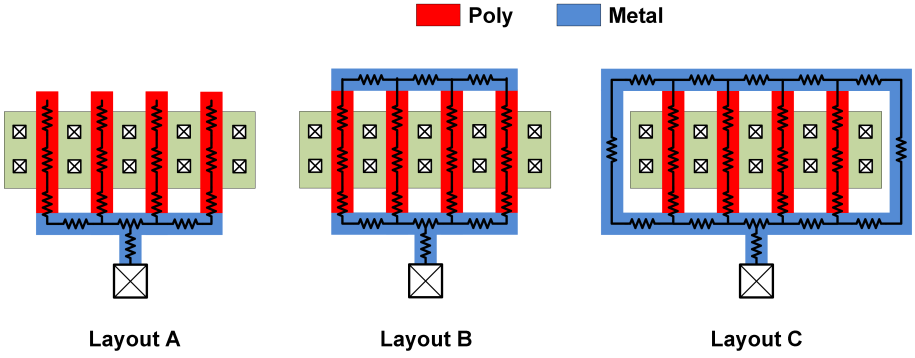


Figure A.1: Layout style for the same number and width of transistor fingers

does not reduce the gate resistance. With an increase in capacitance due to the extra interconnect metals (reduced f_t, but no significant reduction in gate resistance, the f_{max} of Layout B ends up being even lower than the case with a single gate contact number, Layout A. This short analysis shows that the whole gate interconnect network should be connected and biased at the same gate voltage to reap the full potential of the gate resistance reduction. In addition, even for small metal traces, the interconnection network has a noticable influence on the total parasitic capacitance of the transistor, and will overtake the gate resistance as the dominant factor for f_{max} for transistor layouts with very narrow and numerous fingers.

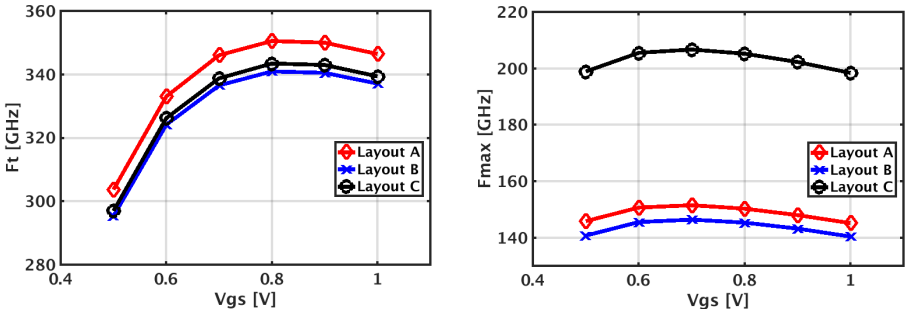


Figure A.2: f_t (a) and f_{max} (b) for the corresponding layout styles depicted in Figure A.1

A.2 Derivation of the asymmetrical double-π inductor model

The conventional inductor model [Lon97] is shown in Figure A.3 and is referred to as the single-π equivalent inductor model.

Combining two single-π models together (Fig. A.4) solves potential problems when one of the ports is connected to ground or supply, and can be reduced to the asymmetrical model shown in Figure A.5.

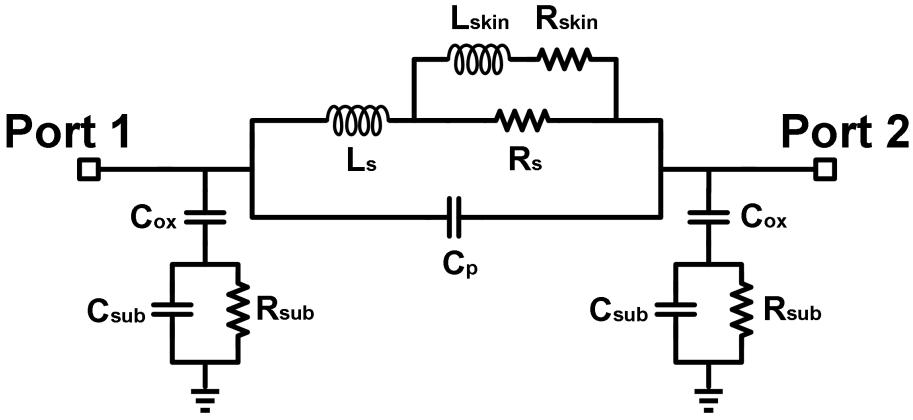


Figure A.3: Equivalent lumped-component model of a single-π inductor

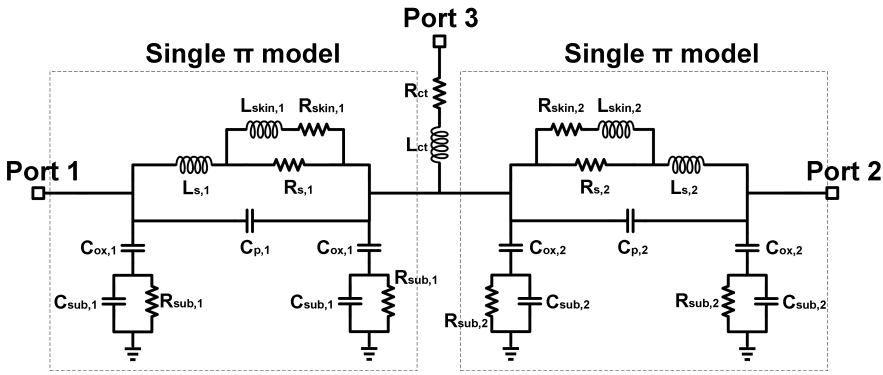


Figure A.4: Equivalent lumped-component model using two single-π inductors connected together, with center tap

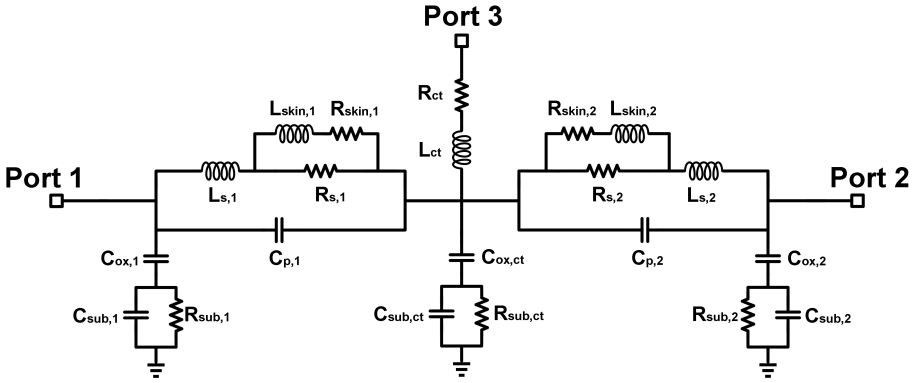


Figure A.5: Resulting asymmetrical double-π inductor model

A.3 High-frequency impact of dummy filling on inductor performance

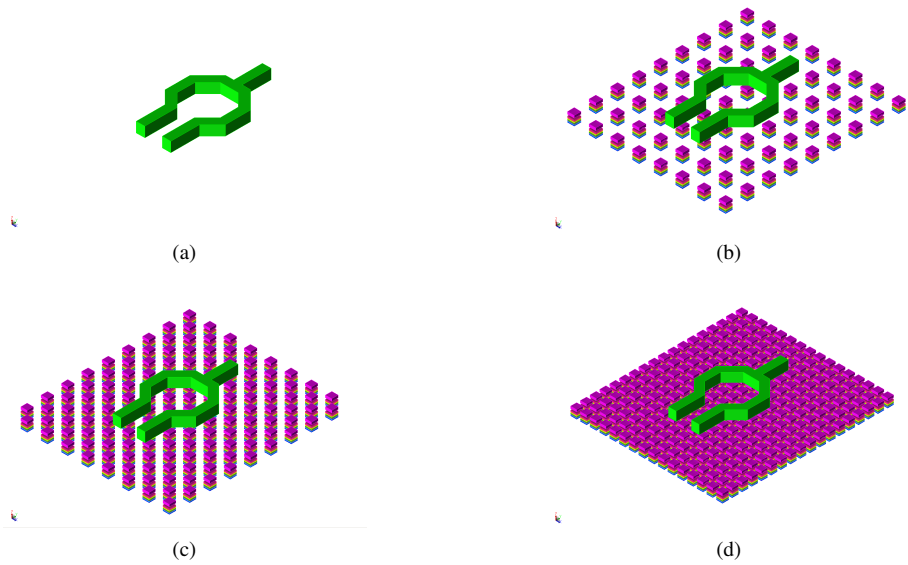


Figure A.6: 3D EM models for inductor simulations at different levels of dummy fill: no dummies (a), 10% (b), 20% (c) and 40% (d) metal density

Density	Dummy size [µm]	L [pH]	Q	Simulation time [s]
No dummies	-	29.92	35.07	4
10%	2.4 x 2.4	29.66	30.25	341
10%	1.2 x 1.2	29.72	30.6	13414
10%	2.4 x 2.4, spiral	29.66	29.59	356
20%	2.4 x 2.4	29.34	26.42	3762
30%	2.9 x 2.9	29	23.18	8403
40%	2.4 x 2.4	28.82	20.62	24111
40%	4.8 x 4.8	28.35	20.29	869
No dummies	-, no substrate	23.26	27.27	-
30%	2.9 x 2.9, no substrate	22.35	18.76	7711

Table A.1: Table with L, Q and simulation time for several dummy filling densities and sizes, evaluated at 200GHz. Mesh size based on highest frequency (750GHz)

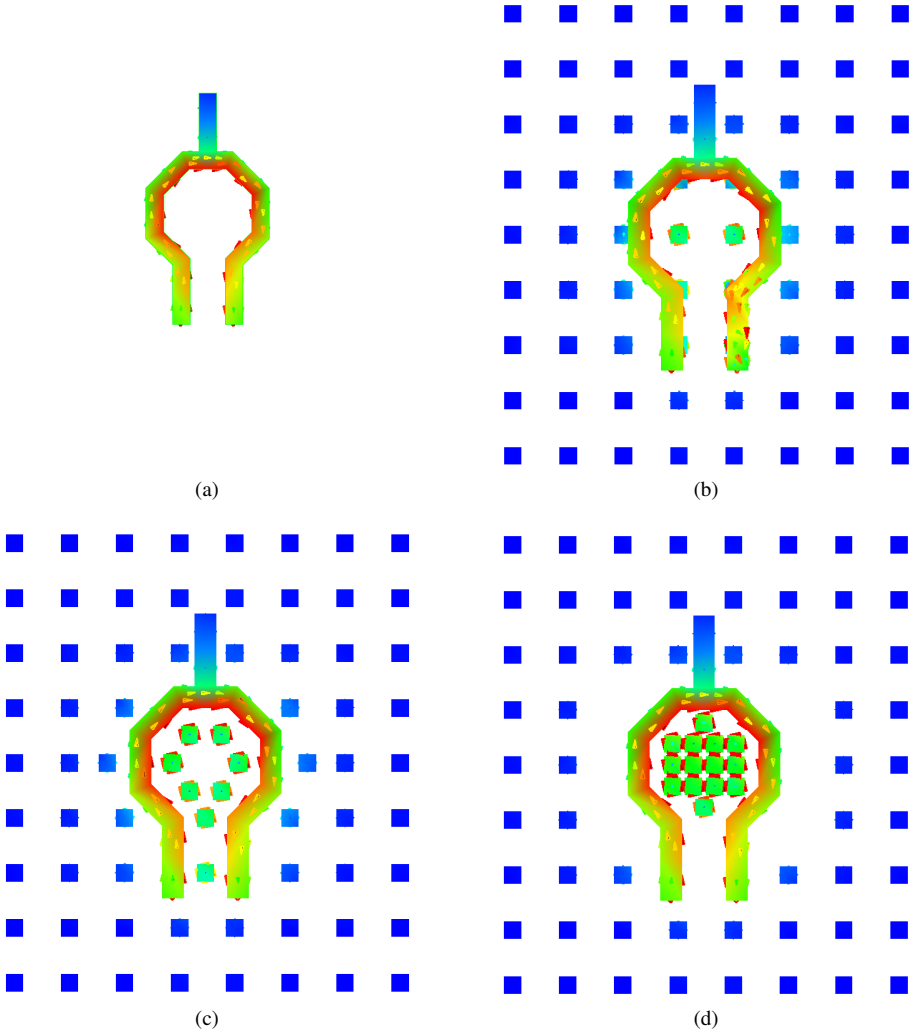


Figure A.7: Current distribution in the single turn inductor at 200GHz for different 10% density dummy filling strategies

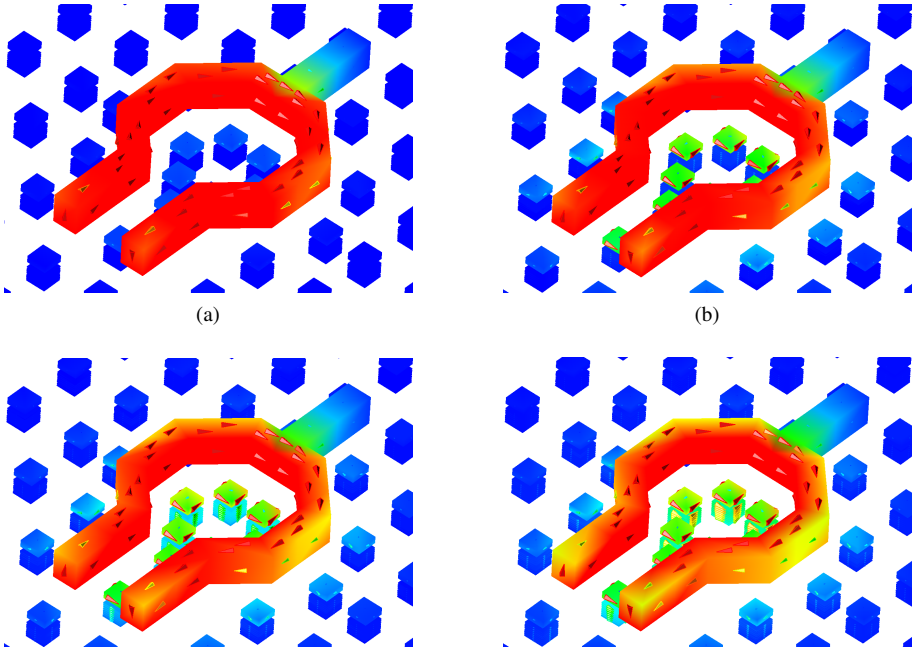


Figure A.8: Current distribution in the single turn inductor and surrounding dummies at 10GHz, 80GHz, 200GHz and 300GHz

A.4 Transmission line Z_0 and γ calculations from S-parameters using ABCD-matrix

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} cosh(\gamma l) & Z_0 \cdot sinh(\gamma l) \\ \frac{sinh(\gamma l)}{Z_0} & cosh(\gamma l) \end{bmatrix} \tag{A.1}$$

$$Z_0 = \sqrt{\frac{B}{C}} \tag{A.2}$$

$$\gamma = \frac{arcosh(A)}{l} = \frac{arcosh(D)}{l} \tag{A.3}$$

The ABCD parameters can be converted from the S-parameters [Fri94] with source impedance Z_{01} and load impedance Z_{02}:

$$A = \frac{(Z_{01}^{*} + S_{11}Z_{01}) \cdot (1 - S_{22}) + S_{12}S_{21}Z_{01}}{2S_{21}(R_{01}R_{02})^{1/2}} \tag{A.4}$$

$$B = \frac{(Z_{01}^{*} + S_{11}Z_{01}) \cdot (Z_{02}^{*} + S_{22}Z_{02}) - S_{12}S_{21}Z_{01}Z_{02}}{2S_{21}(R_{01}R_{02})^{1/2}} \tag{A.5}$$

$$C = \frac{(1 - S_{11}) \cdot (1 - S_{22}) - S_{12}S_{21}}{2S_{21}(R_{01}R_{02})^{1/2}} \tag{A.6}$$

$$D = \frac{(1 - S_{11}) \cdot (Z_{02}^{*} + S_{22}Z_{02}) + S_{12}S_{21}Z_{02}}{2S_{21}(R_{01}R_{02})^{1/2}} \tag{A.7}$$

The capacitance C_{tl} and inductance L_{tl} of a transmission line can be calculated using:

$$C_{tl} = \frac{1}{\omega} \cdot imag\left\{\frac{\gamma}{Z_0}\right\} \tag{A.8}$$

$$L_{tl} = C_{tl} \cdot \frac{B}{C} \tag{A.9}$$

Appendix B

Additions to Chapter 3: Antennas and IO

B.1 Maxwell equations on electromagnetism

And God said ...

$$\nabla \cdot D = \rho_v \tag{B.1}$$

$$\nabla \cdot B = 0 \tag{B.2}$$

$$\nabla \times E = -\frac{\partial B}{\partial t} \tag{B.3}$$

$$\nabla \times H = \frac{\partial D}{\partial t} + J \tag{B.4}$$

... and there was light.

The (simplified) Maxwell equations come from a series of publications made between 1861 and 1865 by James C. Maxwell, which form the foundation of the classical electromagnetism theory. They combine and relate the work and discoveries of other scientists (Ampere, Faraday, Gauss, Thomson, ...) to describe the theory of electromagnetism in twenty equations [Max65], which were later simplified and reduced to four (Equations B.1 - B.4) by Oliver Heaviside.

B.2 Free-space dipole graphs

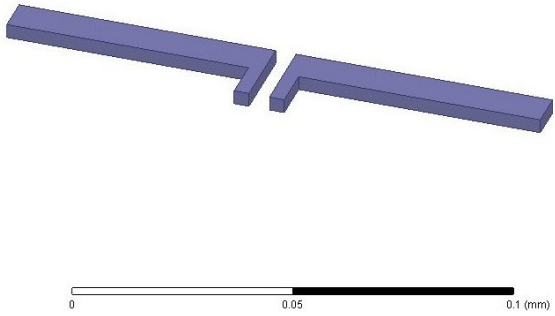


Figure B.1: 3D simulation model of a free-space half wave dipole antenna

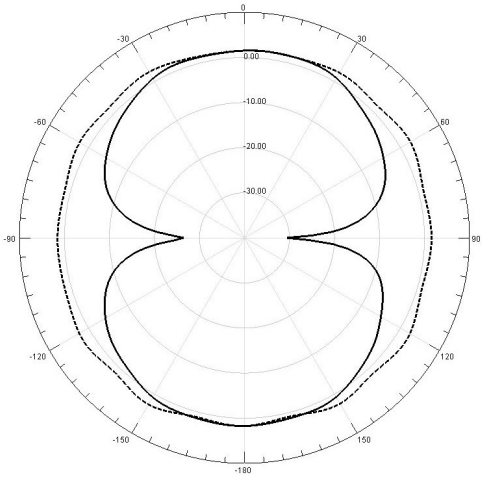


Figure B.2: 2D radiation pattern (gain, dB) of a free-space half wave dipole antenna (ϕ angle: dashed = 0°, solid = 90°)

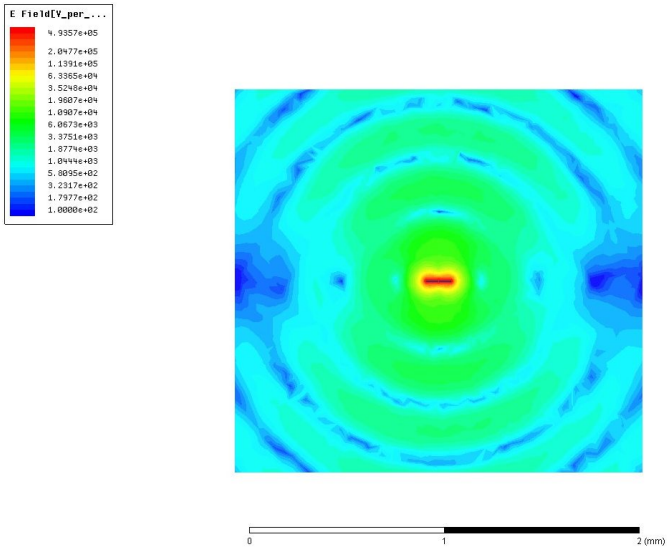


Figure B.3: E-field of a free-space half wave dipole antenna

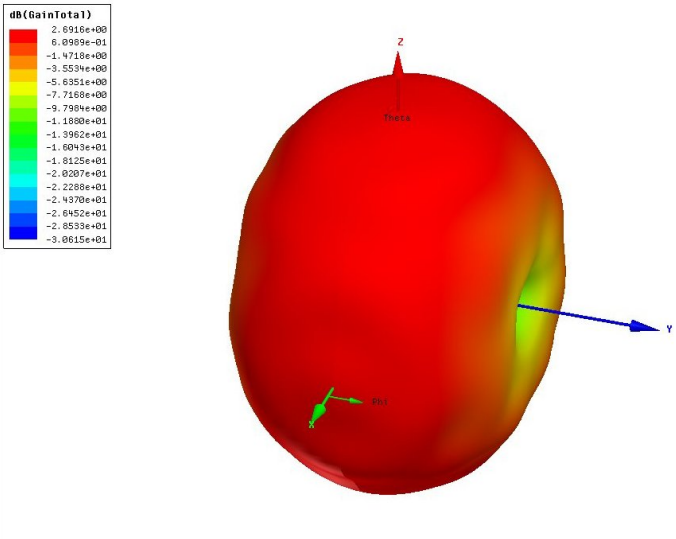


Figure B.4: 3D radiation pattern of a free-space half wave dipole antenna, showing the typical toroid or donut-shaped radiation pattern

B.3 Flipped Patch antenna

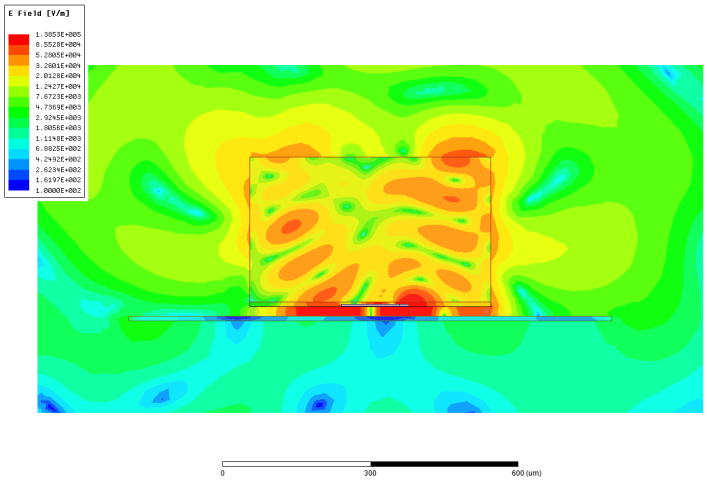


Figure B.5: E-fields in the flipped patch antenna, radiating at 600GHz

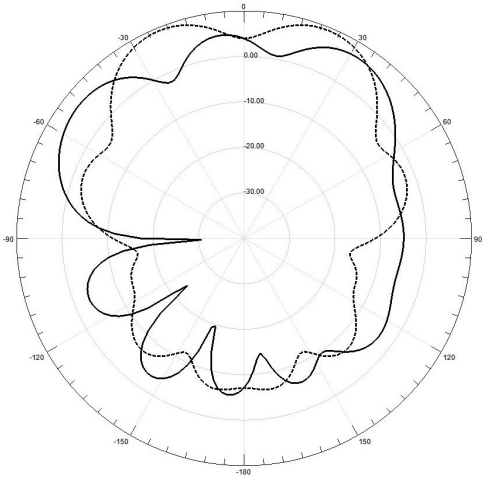


Figure B.6: 2D radiation pattern (directivity, dB) of the flipped patch antenna, operating at 600GHz (ϕ angle: dashed = 0°, solid = 90°)

B.4 Off-chip antenna graphs

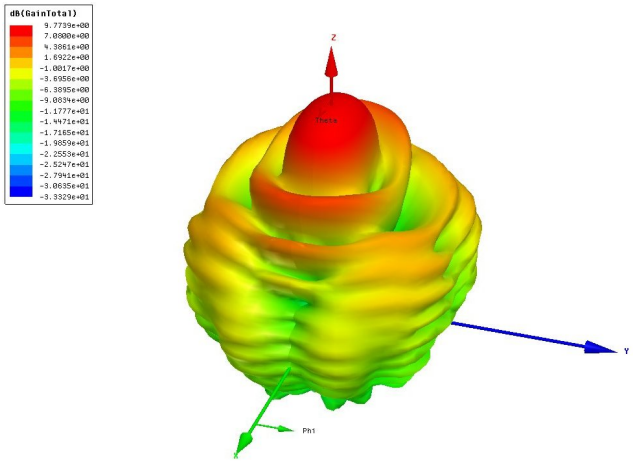


Figure B.7: 3D radiation pattern of a printed horn antenna with reflector (gain, dB)

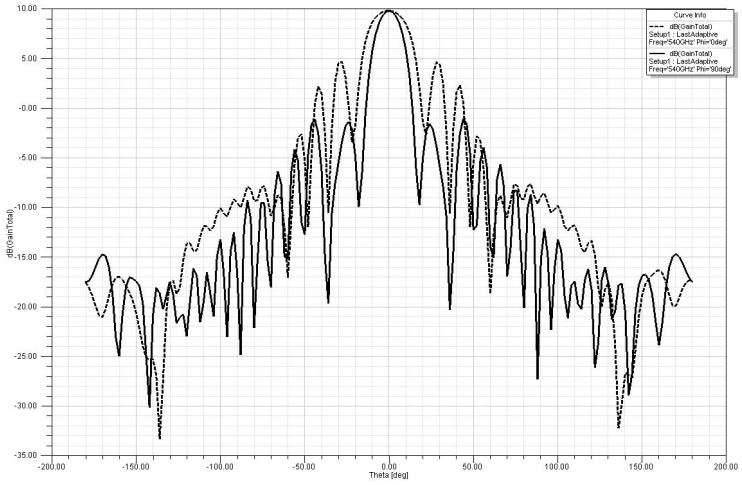


Figure B.8: 2D gain pattern of a printed horn antenna with reflector (ϕ angle: dashed = 0°, solid = 90°)

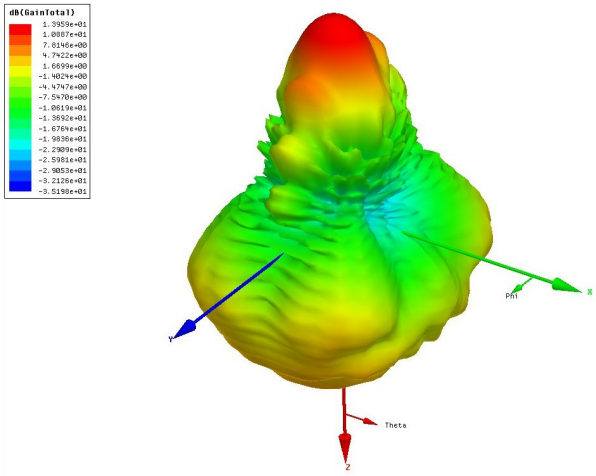


Figure B.9: 3D radiation pattern of a printed horn antenna mounted on the backside of the silicon wafer (gain, dB). Note that the main radiation lobe is in the negative Z-direction

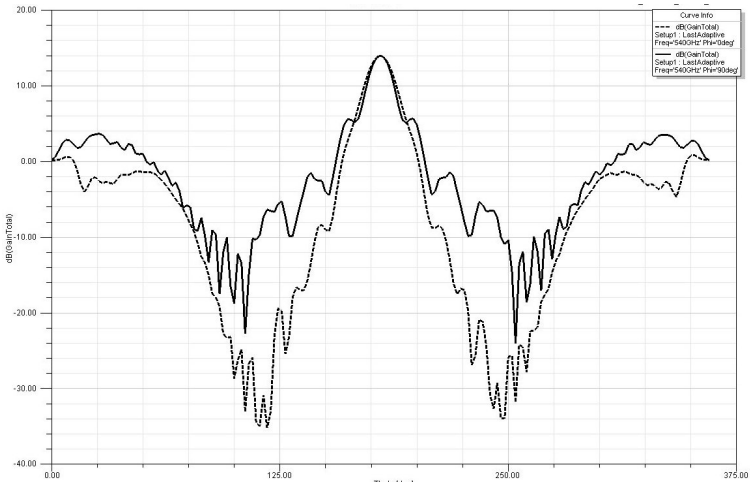


Figure B.10: 2D gain pattern of a printed horn antenna mounted on the backside of the silicon wafer (ϕ angle: dashed = 0°, solid = 90°)

Appendix C

Additions to Chapter 4: THz transmitter circuits

C.1 Volterra series description of a non-linear circuit

The system overview of a Volterra series representation of a non-linear system is shown in Figure C.1. Each H_i block is a Volterra operator, which describes the ith order, frequency-dependent input-output signal relationship. The result of this ith order non-linearity for an input signal $x(t)$ is denoted as $H_i[x(t)]$. The H_1 operator describes the linear behavior of the system, while all higher-order Volterra operators describe the non-linear frequency-dependent behavior.

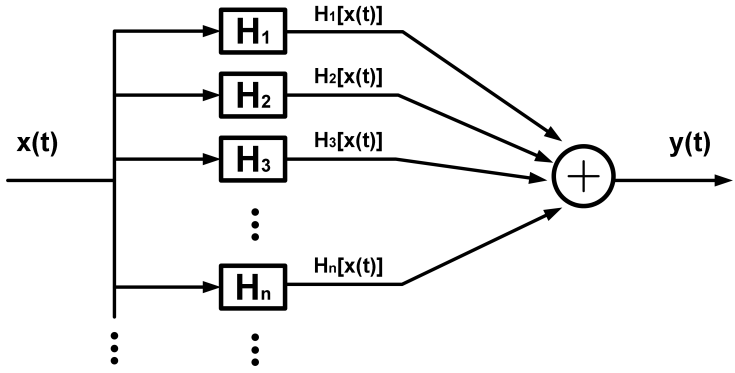


Figure C.1: Schematic overview of a Volterra series representation of a non-linear system

The presence of higher-order harmonics depends on the input signal amplitude: for a very small input signal, the harmonics will not have a significant presence and the

system can thus be reduced to a first order Volterra series, consisting of the first-order operator H_1 (linear behavior). For increasing input amplitude, the amplitude of higher-order harmonics will rapidly increase (as was concluded in Section 4.2.1) and can be added accordingly to the system model with higher-order Volterra operators. An nth order Volterra series will include an n number of Volterra operators, and will therefore be able to model the non-linear behavior of the system up to the nth harmonic of any input signal.

C.2 Individual phases in a N=4-push oscillator

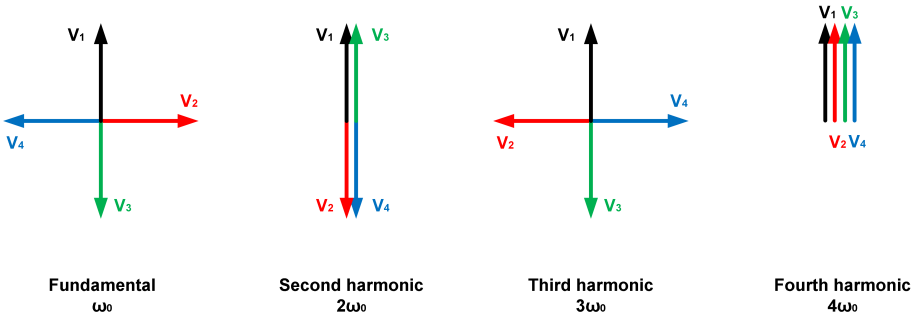


Figure C.2: Phasor representation of the individual output signals at the different harmonics for a N=4-push circuit

Table C.1: Phases of the different output signals at each harmonic for a N=4-push circuit

# / θ	θ at ω_0	θ at $2\omega_0$	θ at $3\omega_0$	θ at $4\omega_0$
Phasor 1	0°	0°	0°	0°
Phasor 2	90°	180°	270°	360° $\rightarrow$ 0°
Phasor 3	180°	360°	540° $\rightarrow$ 180°	720° $\rightarrow$ 0°
Phasor 4	270°	540° $\rightarrow$ 180°	810° $\rightarrow$ 90°	1280° $\rightarrow$ 0°
Σ	0	0	0	4x fourth harm.

C.3 Process variation of UTM and impact on single-turn inductor performance at 200GHz

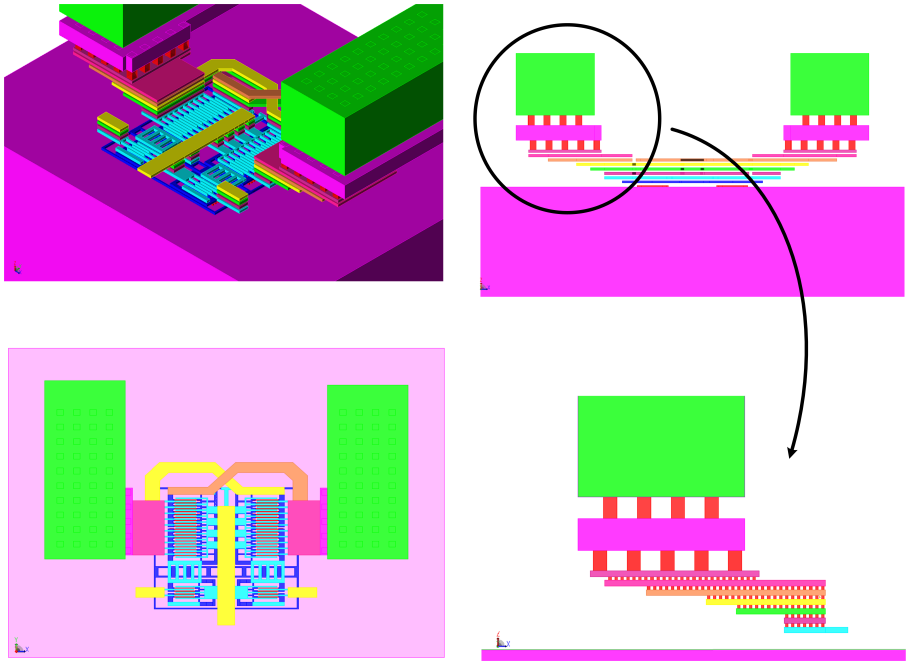
Inductance [pH]	Large W	Nominal W	Small W
Large T	22.53	22.76	22.97
Nominal T	23.74	24	24.25
Small T	24.46	24.85	25.12

Table C.2: Impact of the process variations on the inductance L of a single-turn inductor, for varying width/thickness

Quality factor Q	Large W	Nominal W	Small W
Large T	28.51	27.76	27.23
Nominal T	27.885	27.13	26.6
Small T	27.43	26.67	26.13

Table C.3: Impact of the process variations on the quality factor Q of a single-turn inductor, for varying width/thickness

C.4 180GHz VCO core 40nm CMOS layout close-ups

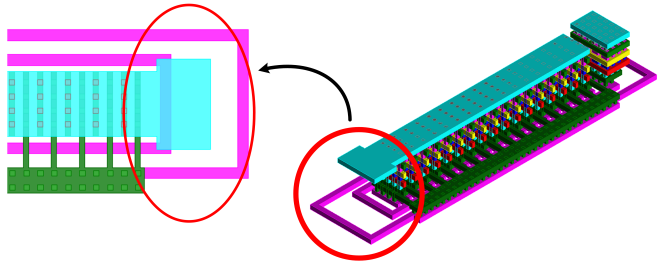


(a) (b)

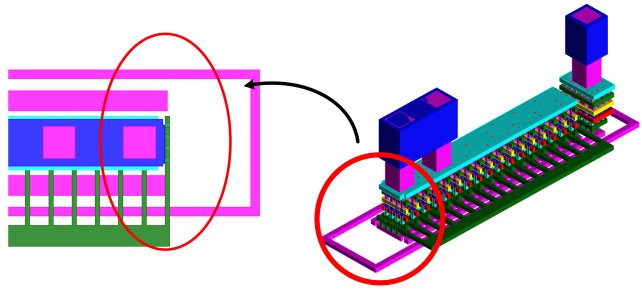
Figure C.3: 3D representation of the cross-coupled VCO core

C.5 THz transistor layout in 28nm CMOS

Illustration of two vertical transistors implemented in 28nm CMOS. Figure C.4a has gate and drain connections up to metal 6, and has a closed double-gate contact loop. The transistor from Figure C.4b contains a via stack up to the first top metal (metal 7), has an open/U-shaped and extra wide double-gate contact connection. While the difference between the two layouts appears to be small, the transistor with the 'open gate' achieves a simulated f_{max} that is 18GHz higher and generates a 9% larger negative resistance when cross-coupled than the 'closed gate' layout, even though the 'open gate' includes interconnection up to a higher metal layer. As the gate resistance R_g remains the dominant parameter for high-frequency performance, the wider M1 gate connection reduces the total distributed gate resistance more than the increase in capacitance to adjacent metals. This shows that when operating at the limit of the transistors' abilities, even small modifications result in pushing the performance a little bit further.



(a)

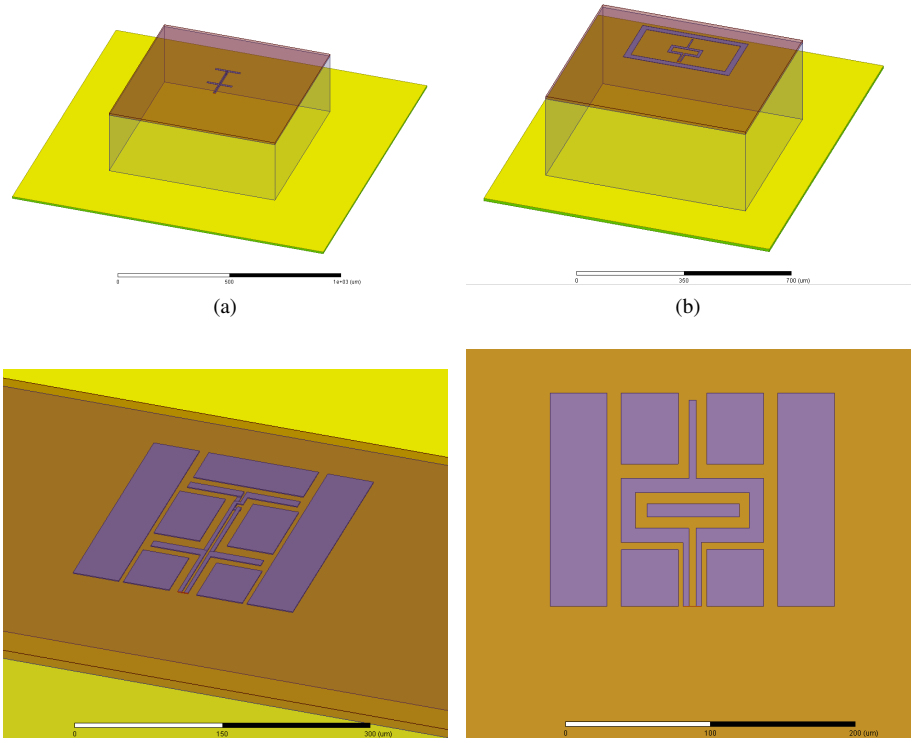


(b)

Figure C.4: Comparison of two layouts of the vertical transistor with (a) and without (b) closed gate contact loop

C.6 Antenna and radiation figures 28nm

C.6.1 3D simulation models of the collinear and folded dipole

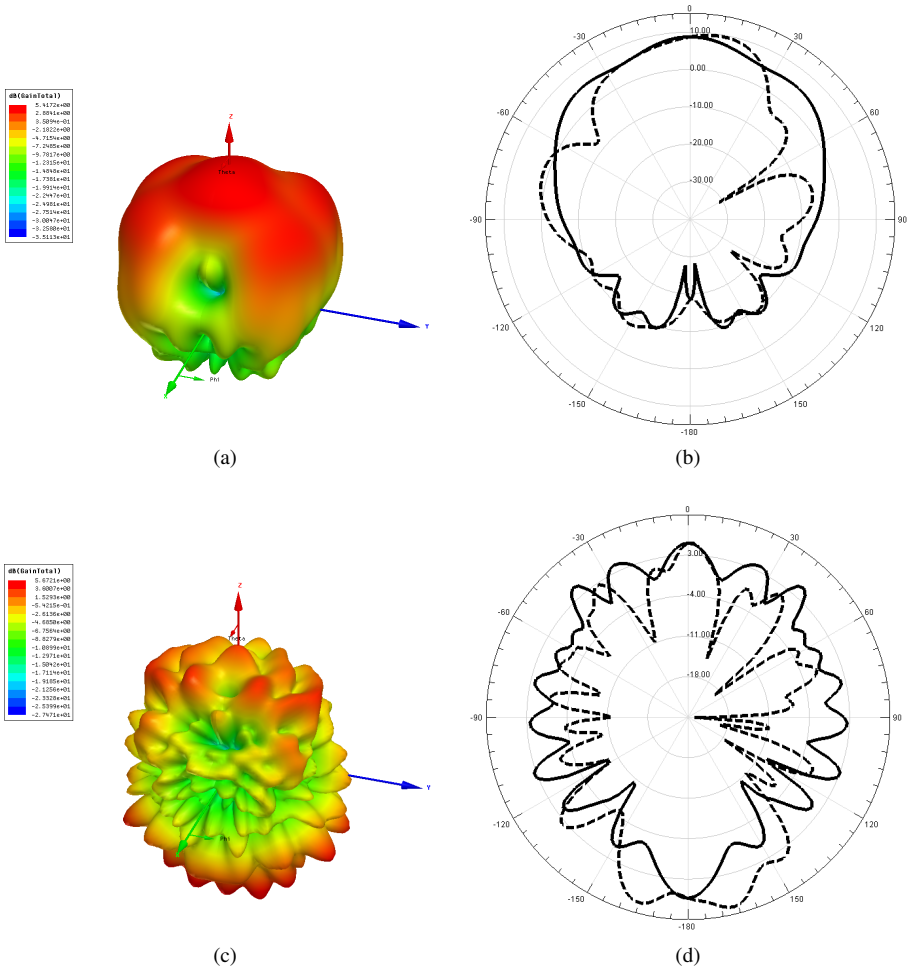


(a) (b)

(c) (d)

Figure C.5: 3D models of the collinear (a and c) and folded dipole (b and d)

C.6.2 Collinear dipole array: 650GHz vs 600GHz



(a) (b)

(c) (d)

Figure C.6: Radiation pattern comparison between the collinear dipole at 650GHz with metal reflector (a and b) and at 600GHz including surrounding metals, but without metal reflector (c and d). 2D radiation patterns on the right show directivity in dB (ϕ angle: dashed = 0°, solid = 90°)

C.6.3 Folded dipole: 630GHz vs 570GHz

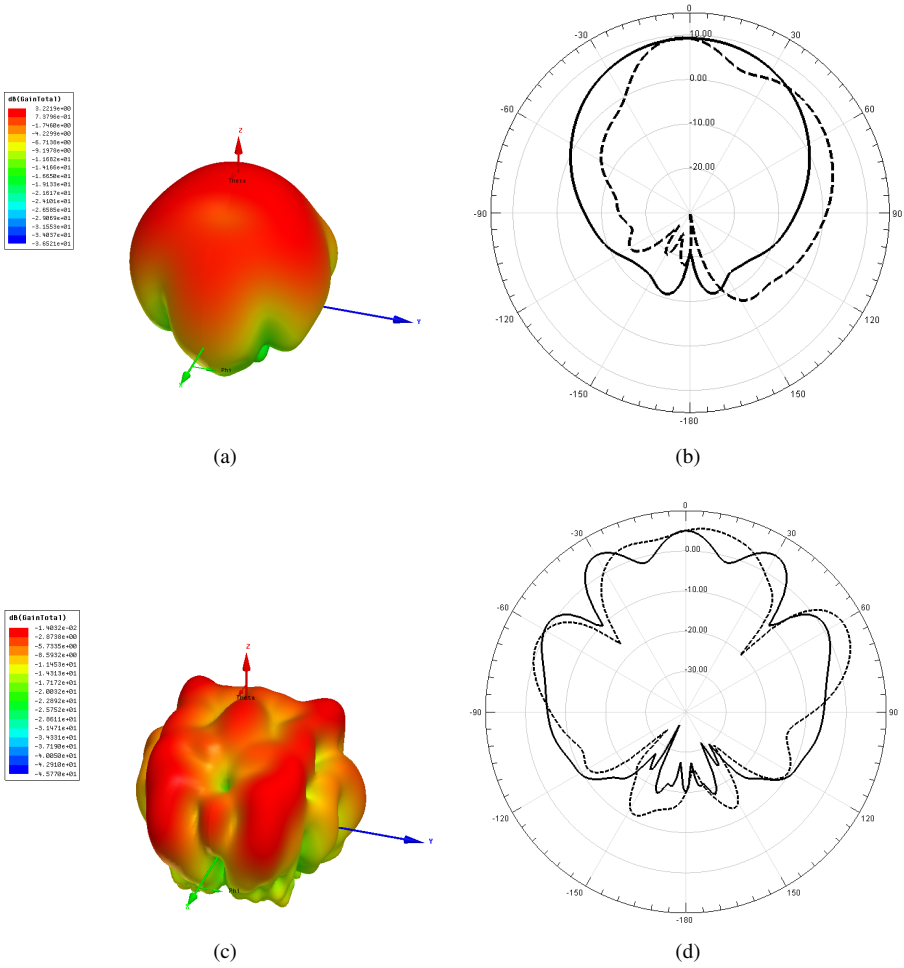
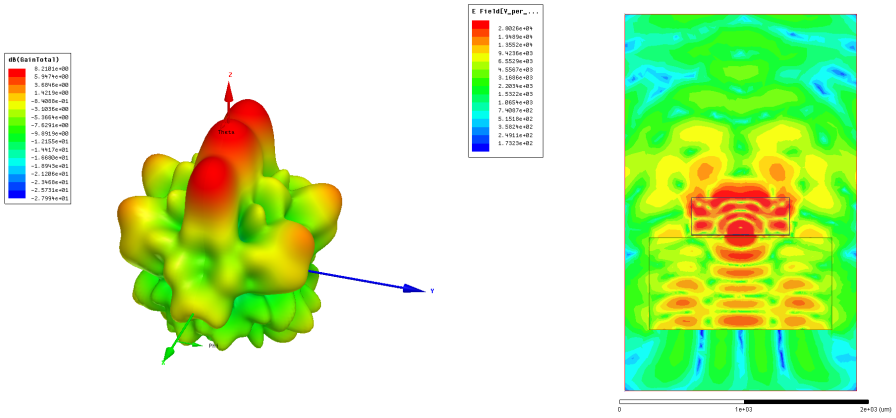


Figure C.7: Radiation pattern comparison between the folded dipole at 630GHz (a and b) and at 570GHz including surrounding metals and metal reflector under the silicon die (c and d). 2D radiation patterns on the right show directivity in dB (ϕ angle: dashed = 0°, solid = 90°)

Appendix D

Additions to Chapter 5: THz receiver circuits

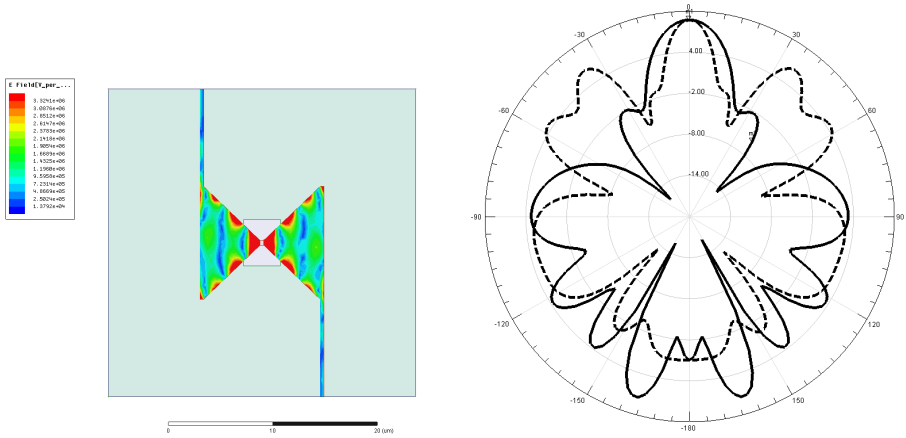
D.1 Flipchip dipole antenna with PCB reflector for SRR



(a) (b)

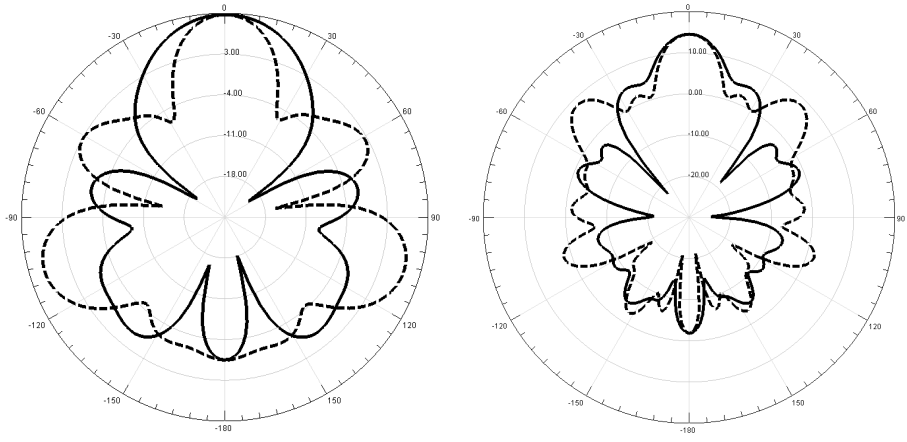
Figure D.1: Flipchip dipole radiation pattern (a) and E-field (b)

D.2 On-chip bowtie antennas for broadband THz detection



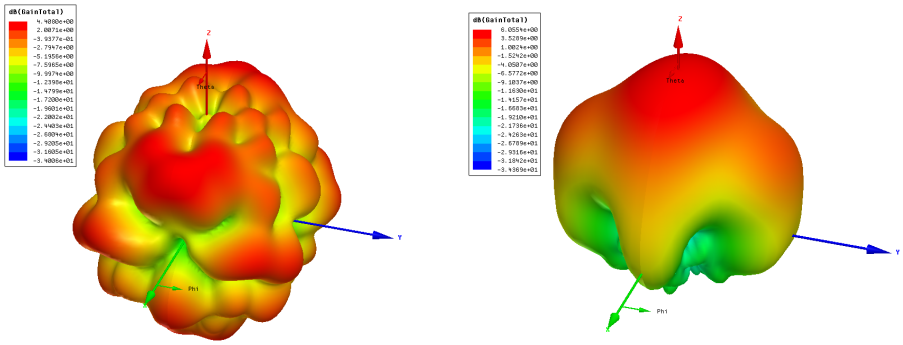
(a) (b)

Figure D.2: Electric field distribution (a) and the simulated directivity (b) of the 30THz bowtie antenna (ϕ angle: dashed = 0°, solid = 90°)



(a) (b)

Figure D.3: Directivity patterns of a 500GHz flipped bowtie (a) and a 900GHz flipped bowtie with PCB reflector (ϕ angle: dashed = 0°, solid = 90°)



(a) (b)

Figure D.4: Bowtie antenna with arm length = 70µm at 800GHz in a flipchip (a) and bondwire with PCB reflector (b) packaging

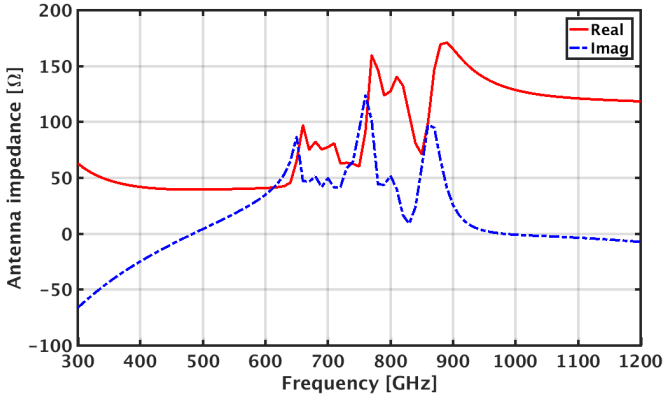


Figure D.5: Simulated impedance of a bowtie antenna with arm length = 50µm and reflector

Biography

Wouter Steyaert was born in Los Angeles, CA, in 1988. He received the Bachelor ('09) and Master of Electrical Engineering ('11) degree from the University of Leuven (KU Leuven). His master thesis was on the design of a wobble-based calibration circuit for temperature-independent oscillators.

During the summer of 2010, he worked as an intern on RF power amplifiers at Toshiba's Research Center in Kawasaki, Japan. Since 2011, he is a research assistant at the ESAT-MICAS group (KU Leuven), working towards a Ph.D in THz CMOS electronics. His main research interests include THz and mm-wave CMOS circuits and their potential applications. He received the Best Design Award in the A-SSCC 2015 Student Design Contest in Xiamen, China. He also won the SSCS Student Travel Grant Award in 2015. Wouter Steyaert regularly serves as a technical reviewer for leading IEEE journals and conferences, including the flagship SSCS Journal of Solid-State Circuits, ISSCC, ESSCIRC and RFIC conferences.

Wouter Steyaert is an active member and former chairman of the IEEE Student Branch Leuven, and served on the board as secretary and vice-chair corporate relations. He organised the 2014 IEEE SB/SSCS Leuven Microsymposium on the topic of Flexible electronics. From 2011 till 2014, he was the ombudsman for the master students in electrical engineering, and served as the ABAP-representative in the POC on both department and faculty level. Wouter Steyaert is a ADS-qualified soft skill certificate holder in creative thinking.

List of publications

Articles in international journals

W. Steyaert, P. Reynaert, "A 0.54 THz Signal Generator in 40 nm Bulk CMOS With 22 GHz Tuning Range and Integrated Planar Antenna", *Solid-State Circuits, IEEE Journal of*, vol. 49, no. 7, pp. 1617 – 1626, July 2014.

V. De Smedt, W. Steyaert, W. Dehaene and G. Gielen, "Wobble-based on-chip calibration circuit for temperature independent oscillators", *Electronics Letters*, vol. 48, no. 16, pp. 1000 – 1001, 2012.

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W. Steyaert, P. Reynaert, "Layout Optimizations for THz Integrated Circuit Design in Bulk Nanometer CMOS", accepted to *Compound Semiconductor IC Symposium (CSICS)*, Oct. 2017.

U. Celik, **W. Steyaert**, P. Reynaert, "A 230.5-238.8-GHz Magnetically Coupled Triple-Push Oscillator with Inductive Tuning for Data Transmission in 45-nm CMOS", in *PRIME 2017, 13th Conference on Ph.D. Research in Microelectronics & Electronics* , June. 2017.

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N. Van Thienen, W. Steyaert, Y. Zhang and P. Reynaert, "On-chip and In-package Antennas for mm-Wave CMOS Circuits", in *Antennas and Propagation (EuCAP), Proceedings of 9th European Conference on*, art. nr. C33.5, April 2015.

W. Steyaert, P. Reynaert, "A 0.54 THz signal generator in 40 nm bulk CMOS with 22 GHz tuning range", in *ESSCIRC (ESSCIRC), 2013 Proceedings of the*, pp. 411 – 414, Sept. 2013.

Seminars, Symposia and Poster Presentations

W. Steyaert, P. Reynaert, "A THz Signal Source with Integrated Antenna for Non-Destructive Testing in 28nm Bulk CMOS", in *Poster presentation at the A-SSCC 2015 Student Design Contest*, Nov. 2015.

W. Steyaert, P. Reynaert, "A 0.54 THz signal generator in 40nm bulk CMOS (and possible applications)", in *Proceedings of imec-KULeuven-CITEF seminar*, Aug. 2014.

W. Steyaert, P. Reynaert, "THz imaging in CMOS at KU Leuven: status and some examples", in *Proceedings of the Wireless Community's 14th Work Meeting: Wireless technologies for remote sensing*, Dec. 2013.

Awards, Grants and Prizes

Asian Solid-State Circuits Conference (A-SSCC) 2015 **Best Design Award** of the Student Design Contest, awarded to W. Steyaert and P. Reynaert.

IEEE Solid-State Circuits Society (SSCS) **Student Travel Grant Award**, awarded to W. Steyaert at A-SSCC 2015.

Book Chapters

P. Reynaert, M. Vigilante, **W. Steyaert** "RF CMOS", book chapter in *Nanoelectronics: Materials, Devices, Applications Volume 1*, 2017.

Supervised Master Thesis

W. Thys, N. Callens, **W. Steyaert** and P. Reynaert "200+GHz Receiver for Gbps communication in 90nm CMOS", 2015 – 2016.

U. Celik, **W. Steyaert** and P. Reynaert "200+GHz coupled oscillator in 90nm CMOS", 2015 – 2016.

G. Caes, **W. Steyaert** and P. Reynaert "200+GHz oscillator in 90nm CMOS", 2015 – 2016.

J. Van Thienen, **W. Steyaert** and P. Reynaert "Sub-Terahertz Pulse-Based LC Oscillator in 45nm CMOS", 2014 – 2015.

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X. Zhang, W. Zhao, **W. Steyaert**, V. De Smedt, W. Dehaene and G. Gielen, "Design of a Self-Calibrating Fully-integrated Clock Reference using a Wobble-Circuit", 2011 – 2012.

MICAS Seminars

W. Steyaert, P. Reynaert, "Excitation and radiation of THz circuits in bulk CMOS technology", in *ESAT-MICAS 2016 Seminars*, Dec. 2016.

W. Steyaert, P. Reynaert, "Sub-millimeter wave CMOS electronics: compact, lens-free and fully integrated THz imaging)", in *ESAT-MICAS 2014 Seminars*, Dec. 2014.

W. Steyaert, W. Volkaerts and F. Ceyssens, "User-generated content for online video-sharing platforms: classification and current state-of-the-art", in *ESAT-MICAS 2014 Seminars*, Nov. 2014.

W. Steyaert, P. Reynaert, "Sub-millimeter Wave Signal Generation in Nanometer CMOS Technology)", in *ESAT-MICAS 2013 Seminars*, May. 2013.

Accompanying reading and music list

Recommended reading
Analog Design Essentials - W. Sansen
RF Microelectronics - B. Razavi
MM-Wave Silicon Technology: 60 GHz and Beyond - A. Niknejad, H. Hashemi
High-Frequency Integrated Circuit - S. Voigenescu
Antenna Engineering Handbook - R.C. Johnson, H. Jasik

Music List
Tomorrow Never Knows - The Beatles
Let It Happen - Tame Impala
Synrise (Soulwax remix) - Goose
Copy of A - Nine Inch Nails
The Social Network OST - Trent Reznor & Atticus Ross
Moan - Trentemoller
Always Something Better - Trentemoller
Rykketid - Trentemoller
Instant Street - Deus
No Eyes - Claptone
Mezzanine - Massive Attack
Head Like a Hole - Nine Inch Nails
Animal Rights - Deadmau5
Purple Haze - The Jimi Hendrix Experience
Little Wing - The Jimi Hendrix Experience
Praise You (Maribou State Remix) - Fatboy Slim
Save a Prayer - Eagles of Death Metal
Do I Wanna Know? - Arctic Monkeys
Air (by Klazz Brothers & Cuba Percussion) - Johann Sebastian Bach
Nocturnes, Op.9 - Frederic Francois Chopin
My Way - Limp Bizkit
Pork and Beans - Weezer
Piano Sonata No. 14 - Ludwig van Beethoven
Ave Maria (by Barbara Bonney) - Franz Schubert
La Femme D'Argent - Air

Balek - Marc Moulin
Television Rules the Nation/Crescendolls - Daft Punk
2 Wicky - Hooverphonic
Loungee - Arsenal
Heroes - David Bowie
Sharp Dressed Man - ZZ Top
Big Calm - Morcheeba
London OST - The Crystal Method
Burst Generator - Chemical Brothers
Hysteria - Muse
Spybreak! - Propellerheads
Paradise Circus - Massive Attack
Inception OST - Hans Zimmer
SexyBack - Justin Timberlake
Session - Linkin Park
Weak - AJR
Smile Like You Mean It - The Killers
True Faith - New Order
You Wanted A Hit (Soulwax Remix) - LCD Soundsystem
Shake It Off - Taylor Swift
Bittersweet symphony - The Verve
Transistor OST - Darren Korb
Zwaar Leven (Official Newbie Song) - Brigitte Kaandorp

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